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Vedic Optimized ALU with a new Approach Urdhva Triyambakam Multiplier

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ABSTRACT

For Fast Operations multiplication is very important in Arithmetic Unit. Available Vedic multiplication hardware has certain limitations, if area is in concern. To reduce these limitations a different approach has been proposed to design the Vedic multiplier with new proposed addition structure. To meet major concern i.e. 'Speed', proposed work need a high speed ALU. The speed of ALU generally depends upon the speed of its multiplication unit used. Proposed multiplication techniques Vedic and tree addition structure gives a very fast and area optimized multiplication method. The proposed model gives ALU algorithm which is efficient in both area and speed.

Keywords:—*EDA, VLSI, Vedic, Wallace, DSP- Digital Signal Processing, ISE, HDL- Hardware Descriptive Language, MAC, CSA, ISE- Integrated Synthesis Environment.*

I. INTRODUCTION

Vedic Mathematics is the ancient way of mathematics which has a various technique of calculations based on around 16 Sutras [8]. There is various multiplication techniques exist now a days at structural and algorithmic level. It has been proved that vedic multiplications the fastest multiplication approach among all other multiplication techniques[1] but there are some different multiplication techniques which are better than vedic multiplication when chip area is in concern[2][4].

By improving the ALU unit one can develop efficient Digital Signal Processor, for which proposed Arithmetic unit appears very useful. One of the major aspects of Vedic mathematics is to execute the tedious calculations in simple manner, even orally computable without use of pen and paper [3][5]. Anyone can do these operations for small numbers and hence Vedic mathematics give methods to solve operations with higher value numbers in a very easy and fast manner. Vedic mathematics has more than one approach for every basic arithmetic computation like multiplication and division. For each operation there is minimum one defined method provided along with few generic methods which are dedicated towards particular cases simplifying the calculations further. Paper [6] and [7] described the Vedic mathematics from staring and discuss all methods and computation. Vedic mathematics provides algorithms to simple the mathematics and that makes it best solution for the problems with speed. Proposed paper work has used the Urdhva Triyambakam sutra for multiplication. Designing is done with the tree addition structure instead of the Conventional Adder, which is required during the Partial Product generation is known tree method, converts the

multi-operand addition into the easy two operand Addition and it takes less time.

II. Proposed Arithmetic Unit

Proposed 16x16 bit Arithmetic Unit is shown in the figure 1.

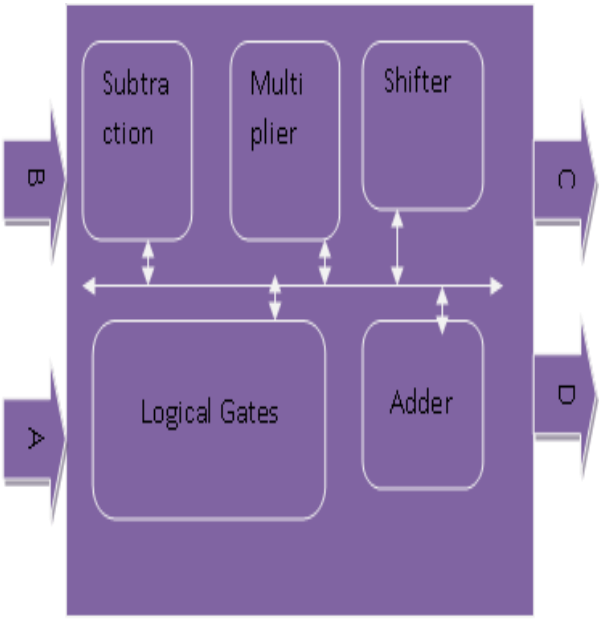

Figure 1. Arithmetic Logic Unit Module

A and B are the two 16 bit inputs for proposed Arithmetic Unit and internal part of the design includes Subtractor, Adder, Multiplier, shifter and logical Gates. Product and Accumulated product are of 32 bit output while subtraction and addition are of 16 bit output. Proposed work never focus on the designing of the adder or subtractor circuits, as known these are not consider as modules which requires large amount of area and power in ALU. But after lots of study it is been found that multiplier is the module which consumes lots of area, time and power, so Vedic multiplication is been developed with new addition tree structure to meet timing constraints.

For proposed approach of multiplication IN1 and IN2 are the two inputs. Now as per Vedic approach it requires 16 logical AND operations with specific crosswise values of given number binary digits.

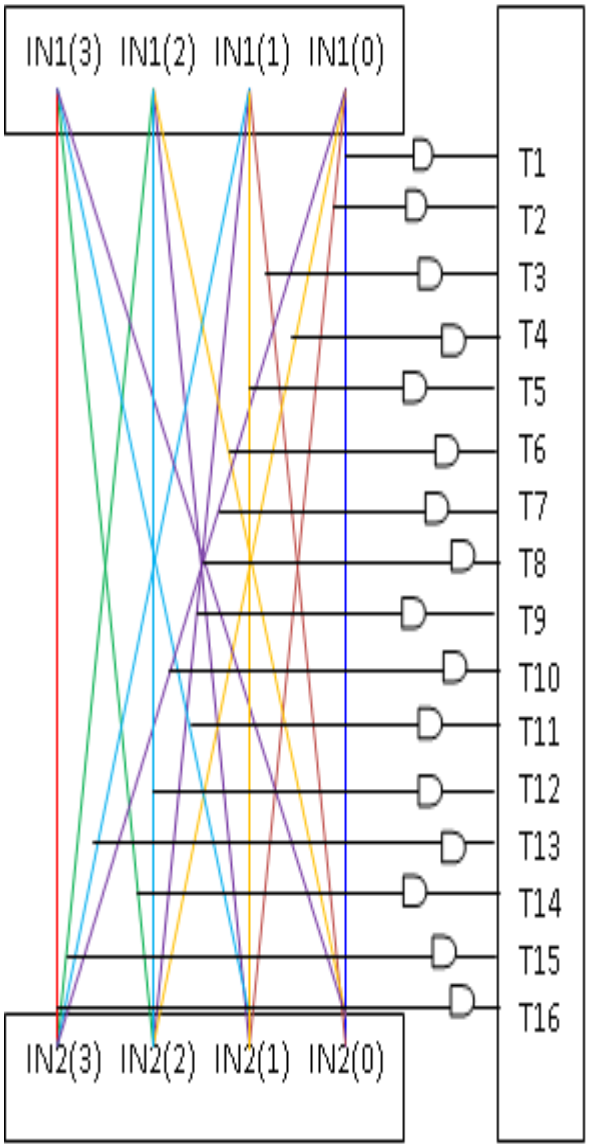

Figure 2: the Vedic Approach

After logical AND cross wise operation obtained values are t1, t2, t3.....t16. To add these values addition structure as shown in figure 3 below.

```
-we need to add-----------------------
 '0'  t16  t14  t11  t7  t4  t2  t1
           t15  t12  t8  t5  t3
                t13  t9  t6
                     t10
---------------------------------------
```

Figure 3: Vedic Intermediate data

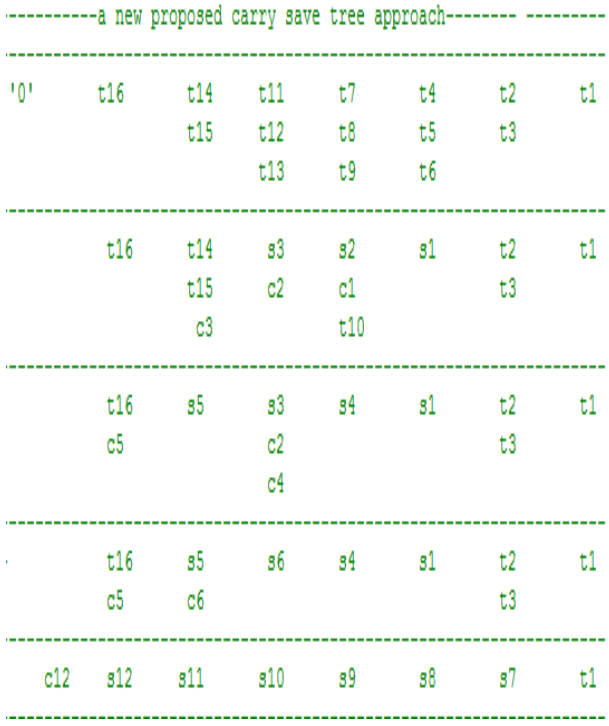

Figure 4: the proposed addition structure

Figure 4 shows the way of performing addition, in this way one can have minimum hardware required as compare with Wallace addition or carry save addition. Proposed addition method requires only 8 full adder and 4 half adder while Wallace addition in this scenario requires total 7 full adders and 8 half adders and carry save adder requires 8 full adders and 7 half adders. It shows that proposed method needs minimum area.

III. RESULTS

Table1: Results Observed for 4x4 Proposed Vedic Tree Multiplier

No of Slices	452
No of 4 input LUT	803
No of bounded IOBs	68
Logical Delay	9.007 ns

Proposed work shows new design for 4 bit Vedic multiplier with the help of Tree adder. Table 1, 2 and 3 given below shows the results for the design of 4x4, 8x8, and 16x16 which has also been implement with new proposed 4x4 Vedic tree multiplier. Figure 5 below shows the simulation results of the ALU module design and it shows the results of subtraction, multiplication and addition.

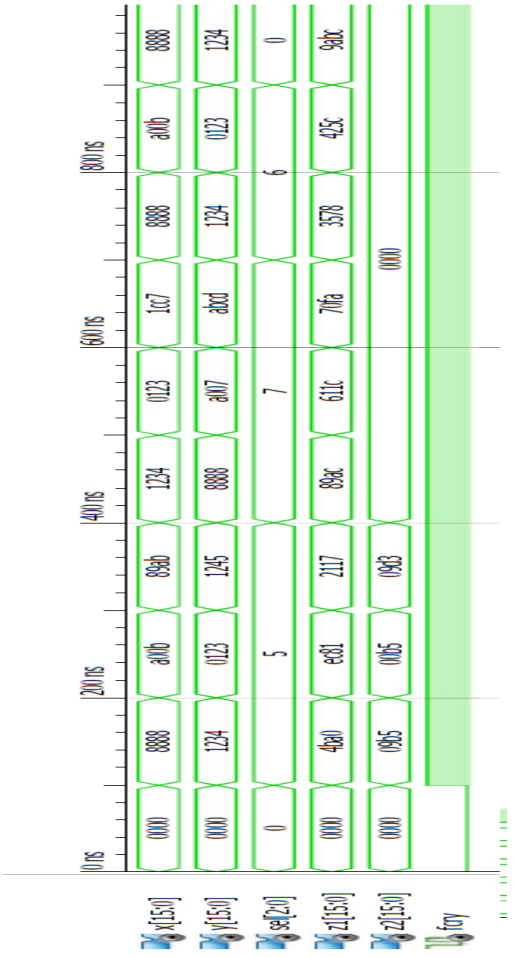

Figure 5: Simulation Results of ALU

Table2: Results Observed for 8x8 Proposed Vedic Tree Multiplier

No of Slices	18
No of 4 input LUT	31
No of bounded IOBs	16
Logical Delay	4.891 ns

Table 3: Results Observed for 16x16 Proposed Vedic Tree ALU

No of Slices	90
No of 4 input LUT	158
No of bounded IOBs	32
Logical Delay	6.468 ns

Table 4: Comparative Results of Proposed Vedic 4x4 with Other Available

	Logical Delay	Slice
Proposed Vedic 4 bit multiplier	4.891 ns	18
Ref4	6.216 ns	27
Ref 5	-	25
Base 3	10.95 ns	20

Table 5: Comparative results of proposed Vedic 8x8 with other available

	Logical Delay	Slice
Proposed Vedic 8 bit multiplier	6.468 ns	90
Ref3	36.563 ns	-
Ref2	15.685 ns	-
Ref1	15.484 ns	-
Ref5	15.518 ns	-

Table 6: Comparative Results of Proposed Vedic ALU with others

Design	Sub design s (If any)	Logical Delay	Slice
Proposed Vedic 4 bit ALU		5.623 ns	18
Base 3 (4x4 ALU)		10.95 ns	20
Design	Sub design s (If any)	Logical Delay	Slice
Proposed Vedic 8 bit ALU		6.655 ns	90
Base 1 (8x8 bit multiplier)	Kartsuba	31.029 ns	-
	Vedic kart-suba	18.695 ns	-
	Optimized Vedic	15.418 ns	-
Base 2 (8x8 ALU)		48.80 ns	-
Base 3(8x8 ALU)		15.52 ns	92

The results have been generated after RTL entry in Xilinx EDA tool. Verification is done on Xilinx ISE and all results have been verified correctly. Above proposed results are batter in terms of area (means less number of Slice) and speed (means less logical delay) in 4 bit ALU and multiplication as compare to base paper number 3.

Above as can observe that proposed results are better in aspect of speed (means logical delay) in 8 bit as compare to base papers 1, 2 and 3.

Proposed work has designed 4 bit Vedic multiplier (original research work) and uses it to design with 16 bit ALU.

Figure 6 shows power of proposed work which is designed with the help of X power analyzer for final validation of design on FPGA.

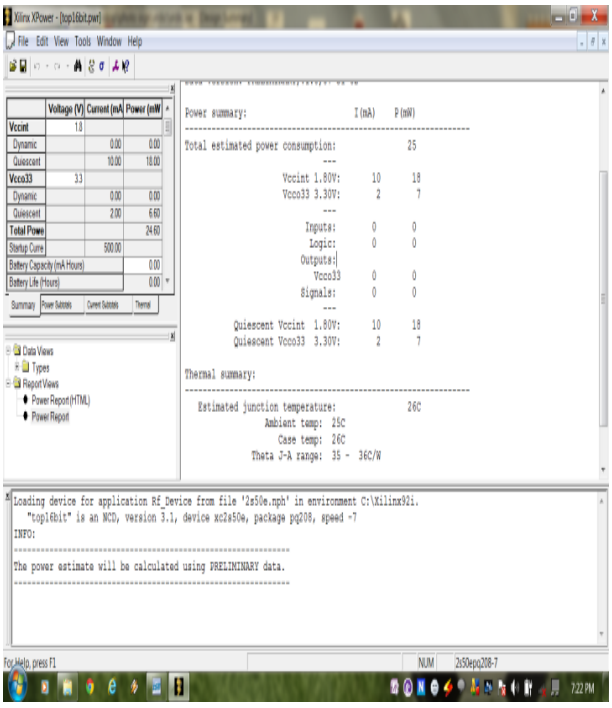

Figure 6: the power report of proposed work

IV. CONCLUSION

Proposed work is a design of 16x16 bit Multiplier which produces better results with respect to the all available Vedic multiplier or another Multiplier. Proposed design makes optimized multiplier and very useful for designing the delay and area optimized ALU, which enhance the Microprocessor, because its performance is dependent on the efficiency of ALU. Proposed design can also be used for make efficient ALU unit of DSP, and hence optimized designs can also be used to design FFT, FIR, IIR, and DFT and their performance is directly dependent on the speed of ALU unit.

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