Volume 1, Issue 4, October 2014 ISSN: 2348-8565 (Online)
International Journal of Modern Engineering and Research Technology
Website: http://www.ijmert.org Email: editor.ijmert@gmail.com

An Implementation of RISC Processor for DSP Applications

Shaily Agrawal
Research Scholar
Takhshshila Institute of Engineering and technology, Jabalpur (M.P.) [INDIA]
Email: juhi1896@gmail.com

Shadma Pragi
Assistant Professor
Department of Electronics and Communication
Takhshshila Institute of Engineering and technology
Jabalpur, (M.P.) [INDIA]
Email:shadmapragi@takshshila.org

ABSTRACT

Microprocessor is a general purpose IC (Integrated Circuit) which simply follows the instructions given to it, and the instructions set for the different microprocessors are different and designed such a way that it can perform required type of computations. Proposed model is a new RISC (Reduced Instruction Set Computing) processor architecture for DSP and it has FSM (Finite State Machine) with new instruction set and RISC feature like executing every instruction in one cycle. Proposed model has use Xilinx ISE 12.2 ISE software for designing all modules. Each module has been tested and verified with all possible instruction which are been supported by proposed design. The proposed architecture of processor requires less area and higher speed as compare with the other existing RISC architecture available.

Keywords:— *ALU, ISE, CISC, FPGA, microcode, RAM, op-code, RISC, SHARC*

I. INTRODUCTION

A Digital Signal Processor (DSP) is a microprocessor particularly to process the digital signals. It has a specialized architecture which is perfect for the fast operational requirement of digital signal processing. A Digital Signal Processor (DSP) is particularly for those applications that cannot tolerate delays because the main feature of DSP is to process the data in real time.[2] Digital Signal Processors take a digital signal and improves the quality of that signal. There are many different kinds of programmable digital signal processors like image signal processor, radar processor, pixel processor, piccolo processor ARM versatile cortex processor. The most common sizes for RAM are 24 kb, 64 kb and 125 MB. There are digital signal processors with RAM sizes up to 1 GB.

RISC processors are generally needed for some specific applications.[3] The concept of ASIP approach of 8 bit processor for small scale system was having isolated memories for OPCODE, immediate operands and data.[1] But now the proposed model is specific for DSP application and concern about execution of fast DSP operations. A new instruction set is also prepared for proposed model, where as in [1] 8085 instruction set was used.

II. PROPOSED ARCHITECTURE

This proposed Design is of 16 bit DSP Processor using Verilog HDL, the designed module will be synthesized using Xilinx ISE 9.1i Web pack,[4] and the verification will be done on ISE simulator, and for validation the design module will be implemented on Array) Vertex-4. [11,12]. Figure-1 shows proposed architecture, In proposed model Xilinx FPGA[5] (Field programmable Gate there are mainly three memories for specific

task MEM1, MEM2, and MEM3. Memory 1 is further divided into 3 parts. In each part different signals are stored. Memory 2 is used to hold the result. The result can big enough therefore MEM2 is divided into 2 parts to store LSB and MSB of result respectively. MEM3 is used to store the OPCODE, address of the signals which are stored in MEM1 and also stores the amount of shifting. Registers are there for holding temporary data during the execution of program**.**

CU (control unit) is CU is FSM based design used for fetching[7] the instruction from MEM2 and extract OPCODE and operands from instruction, then after decoding[10] the OPCODE it generate required OPCODE for ALU module, here one can say CU acts as the master for ALU and it gives order to the ALU. CU read the signals from MEM1 as per the decoded OPCODE, read the results generated from ALU and also write back it into the MEM2.

ALU has three major modules Adder-Subtractor, shifter and Multiplier.[6] The multiplier is used for the multiplication of two numbers. So for multiplication iteration based Mitchell method is used. Mitchell multiplication is good for dealing with floating numbers. The floating numbers in proposed work has 6 binary place. let's have an example if we want to write 13.75 it would be 0000001101.110000.

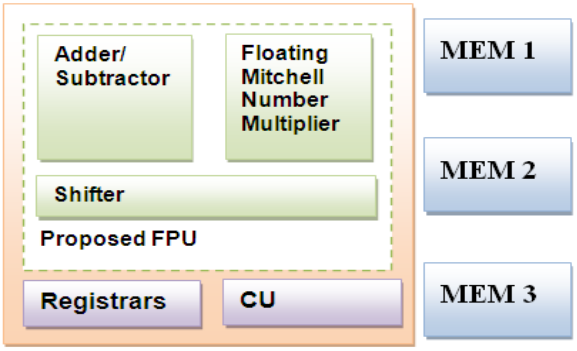

Figure 1: proposed RISC cum DSP processor architecture

Table 1: OPCODE of Proposed Design

Multiple operation + multiplication + add + sub + (0 no shift+1 shift)+(0 right shift one,1left shift one)			
OPCODE	**HEX**	**Operation**	**Mne-monics**
0100_00XX	40	Multiplication only	MUL
1110_00XX	E0	Multiplication and addition	MAD
1101_00XX	D0	Multiplication and subtraction	MAS
0100_10XX	48	Multiplication and shift right signal one	MRS
0100_11XX	4C	Multiplication and shift left signal one	MLS
0010_00XX	20	Addition only	ADD
0010_10XX	28	Add with right shift signal one	ARS
0010_11XX	2C	Add with left shift signal one	ALS
0001_00XX	10	Subtraction only	SUB
0001_10XX	18	Sub with right shift signal one	SRS
0001_11XX	1C	Sub with left shift signal one	SLS
0000_10XX	08	Shifting only right signal one	RS
0000_11XX	0C	Shifting only left signal one	LS
1110_10XX	E8	Multiplication addition right shift signal one	MAR
1110_11XX	EC	Multiplication addition left shift signal one	MAS
1101_10XX	D8	Multiplication subtraction right shift signal one	MSR
1101_11XX	DC	Multiplication subtraction left shift signal one	MSL

This paper also proposed a new RISC Instruction set for DSP application along with its OPCODE as shown in table 1.

OPCODE designs are mainly used for DSP applications. Multiple operations like addition, subtraction, multiplication and shifting can be executed in single instruction. Generally RISC processors[8] execute single operation in single instruction but by proposed model it is possible to execute multiple operation in single instruction.

III. Result & Simulation

The proposed core architecture has been designed and simulated with the help of Xilinx ISE software. The result is as shown below.

Table 2: Logic Utilization

Target FPGA family Vertex 4	
Number of slices	184
Number of LUT	329
Number of slice flip flop	143
Logical time required	3.683ns
Max freq.	271.517 Mhz

Table 2 shows the observed results for the Proposed DSP processor.

1 slice = 2 LUT (Look Up Table) and 1 Flip Flop and 1 LUT = 4 input/ output PLA (Programmable Logic Array). In proposed model less slices are used it means number of LUTs and flip flops are less. Therefore less hardware is required. The maximum frequency is 271.517Mhz which is very high in proposed model.

Table 3: Comparative Analysis

Target FPGA family Vertex family	**Propo-sed model**	**Base [2]**	**Base [4]**	**Base [6]**	**Base [8]**	**Base [9]**
Number of slice	184	-	-	-	428	448
Number of LUT	329	-	624	1462	-	-
Number of slice flip flop	143	-	-	-	-	-
Logical time require	3.683 ns	-	-	10.8	-	-
Max freq.	271.517 Mhz	13 Mhz	253.8 Mhz	-	-	96.33 Mhz

Table 3 above shows the comparative result with five research papers [2] [4] [6] [8] [9]. As table shows the frequency is 13MHZ only in [2] and 271.57MHZ in proposed model, which is higher than other reference papers. Number of LUTs which are used in [6] are 1462 and only 329 are used in proposed model which means less hardware is required in proposed model.

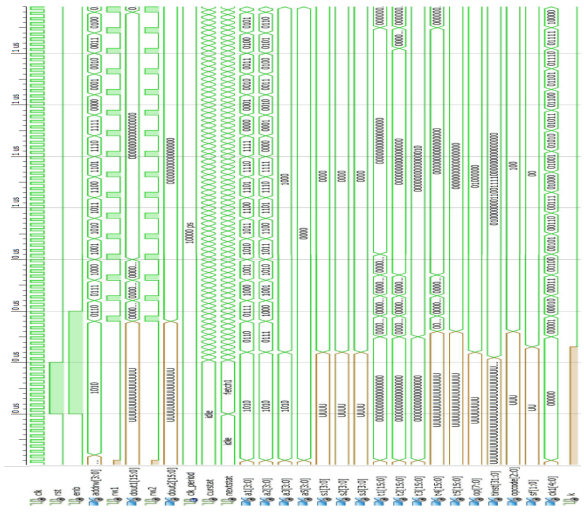

Figure 3 1.Simulation of MUL instruction with signals (6,1,9,2,8)

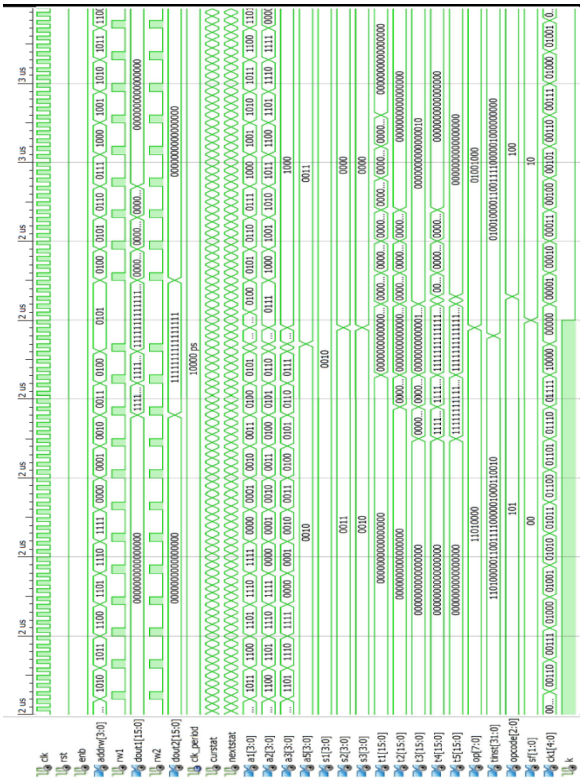

Figure 3 2S i mulation of ADD instruction with signals (6,1,9,2,8)

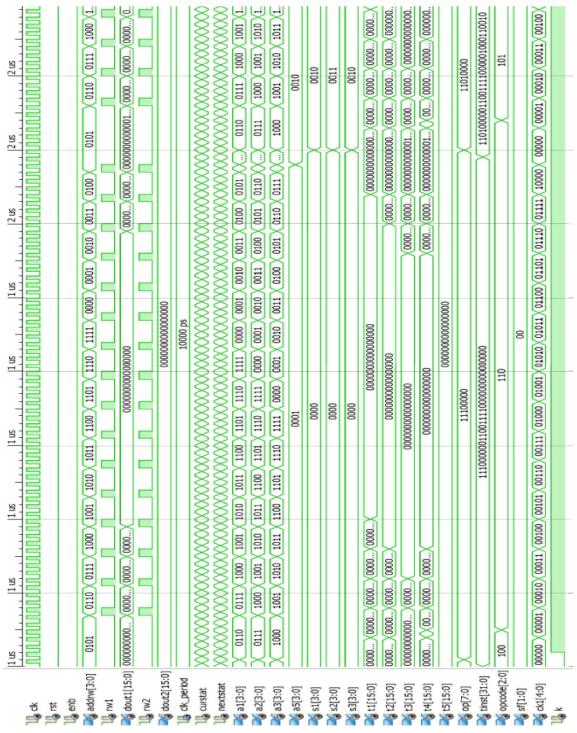

Fig 3 3.Simulation of SUB instruction with signals) (6,1,9,2,8

Figure 3.1 3.2 and 3 3.shows the simulation observed for the proposed work and it shows execution of MUL, ADD and SUB instruction for instruction set with two signals having 5 bit length and having different starting positions. The simulation is observed for all the OPCODES shown in table 1 but this paper shows simulation of MUL, ADD and SUB only.

IV. CONCLUSION

The proposed work is a new RISC architecture based DSP processor[12] and it can be concluded by observing results in table 2 and 3 that proposed architecture is the best among all the existing work in terms of *area* and *speed* both. The work is a FSM based design and implemented and verified on Xilinx EDA tool. The verification is done with the help of ISE simulator of Xilinx and tested for every OPCODE of table 1.

REFERENCES

[1] Shaily Agrawal, Sadhma Pragi. An ASIP approach of 8 bit processor for small scale application, International Journal of Modern Engineering and Management Research, Volume 2, Issue 1, pp 56-60, March 2014,

[2] Tasnim Ferdous Design, Synthesis and FPGA-based Implementation of a 32-bit Digital Signal Processor, International Journal Of Scientific & Engineering Research, Volume 3, Issue 7, July-2012

[3] Ryszyard gal, adma golda, maciej frankiewics, andrzej koz, FPGA implementation of 8 bit RISC Microcontroller for Embedded systems, MIXDES 2011, technical university of Lods,

[4] Aneesh. R, Jiju. K,Design of FPGA based 8-bit RISC controller IP core

using VHDL, India Conference (INDICON), 2012 Annual, IEE, 7-9 Dec. 2012,

[5] Ranganadh Narayanam, Artyom M. Grigoryan, Parimal A. Patel, Bindu Tushara D., Implementation and performance evaluation of paired transform based Faster FFT: Grigoryan FFT on Xilinx FPGAs and TMS DSPs using MATLAB: SIMULINK and CC Studio, International Journal of Scientific & Engineering Research, Volume 4, Issue 8, August-2013

[6] Sunitha M S, Bharat G Hegde, Deepaka kumar N Hegde, design and comparison of risc processors using different alu architectures, international Journal of Innovative Research in Science, Engineering and Technology Vol. 2, Issue 7, July 2013

[7] Mrs. Rupali S. Balpande., Mrs. Rashmi S. Keote., Design of FPGA based Instruction Fetch & Decode Module of 32-bit RISC (MIPS) Processor. 2011 International Conference on Communication Systems and Network Technologies, IEEE.

[8] Yanfen Chen,Wuchen Wu,Ligang Hou,Jie Hu, VLSI & Integrated System Lab. Design and Implementation of 8-bit RISC MCU, Microelectronics and Electronics (PrimeAsia), 2010 Asia Pacific Conference on Postgraduate Researc, 22-24 Sept. 2010, IEEE.

[9] Tomas Balderas-Contreras, Rene Cumplido, Claudia Feregrino-Uribe, On the design and implementation of a RISC processor extension for the KASUMI encryption algorithm, Computers and Electrical Engineering 34 (2008) 531–546, ScienceDirect and Elsevier.

[10] Chien-Hsuan Wu, Chin-Yu Huang, and Jun-Ru Chang, Application-Specific RISC Architecture for ITU-T G.729 Decoding Processing, TENCON 2006. 2006 IEEE Region 10 Conferenc, 14-17 Nov. 2006

[11] http://www.xilinx.com/support.htm

[12] Amit Kumar Singh Tomar, Rita Jain, 20-Bit RISC & DSP System Design in an FPGA, publication in Computing in Science and Engineering,DOI journal, 2013 IEEE.

* * * * *