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Hardware efficient Multiplier using Resource Reuse

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ABSTRACT

This paper proposed an area efficient low power multiplier using resource reuse technique. The proposed design uses efficient design of half and full adder circuits which uses less number of logic gates. As the binary multipliers for n x n bits requires n rows of adder circuit to manipulate the product term. The proposed design requires only 3 rows of adders and intermediate product terms are stored in the memory elements (flip flop). As flip flops takes less area and consume less power as compared to adder circuit (combinational circuit). This technique is applied for 8x8 multiplication and results are compared with standard binary multiplier.

Keywords:—*Low Power, Multiplier, Switching Delay, low area, resource reuse*

I. INTRODUCTION

Multipliers play an important role in today's digital signal processing and various other applications. With advances in technology, many researchers have tried and are trying to design multipliers which offer either of the following design targets – high speed, low power consumption, regularity of layout and hence less area or even combination of them in one multiplier thus making them suitable for various low power and compact VLSI implementation.

It is well known that Multipliers consume maximum power in DSP computations[1]. Hence, it is very important for modern DSP systems to design low-power multipliers to reduce the power dissipation. In low-power multiplier design, many researcher experiments & find out results on the reduction of the switching activities[2] have been published. Besides that, a simple and straightforward approach[3] for low-power multiplier is to design a low-power Full Adder to reduce the power dissipation in an array multiplier. The other designs are proposed to reduce the power dissipation in a multiplication operation by interchanging dynamic operands[4] or using partially guarded computation[5]. Furthermore, to minimize power dissipation architectural modification can be used via row bypassing[6] or column bypassing[7] techniques. Based on the concept of theory row and column bypassing techniques for the reduction of the power dissipation, a low-power 2 - dimensional bypassing based multiplier[8] and a low-power row-and- column bypassing-based multiplier [9] are further proposed. However, the introduction of the extra bypassing circuit decreases the ability of minimize the power dissipation, and it also induces extra delay in the circuit.

In array multiplier n number of full adder layers are required, where n is the size of the architecture. In this work we have used only

three layers of full adders to implement the complete design, this will reduce the area requirement and it will also reduce the power consumption of the design.

II Related work

The multiplication of two 4 bit numbers is shown in the Figure 1.

			Y=	Y3	Y2	Y1	Y0
			X=	X0	X0	X0	X0
				Y3X0	Y2X0	Y1X0	Y0X0
			Y3X1	Y2X1	Y1X1	Y0X1	
		Y3X2	Y2X2	Y1X2	Y0X2		
	Y3X3	Y2X3	Y1X3	Y0X3			
P7	P6	P5	P4	P3	P2	P1	P0

Figure 1: 4 X 4 Array Multiplication

An example of above multiplication process is shown in Figure 2:

			Y=	1	0	0	1
			X=	1	1	1	0
				0	0	0	0
			1	0	0	1	
		1	0	0	1		
	1	0	0	1			
0	1	1	1	1	1	1	0

Figure 2: 4 X 4 example of array multiplication

Generally AND & OR gates are used to generate the Partial Products, PP, If the multiplicand is N-bits and the Multiplier is M-bits then there is N* M partial product. The way that the partial products are generated or summed up is the difference between the different architectures of various multipliers.

For CMOS circuits design, the power dissipation can be divided in two categories as static power dissipation and dynamic power dissipation. In general, static consumption is from the leakage current and dynamic consumption is from the switching transient current. For static power dissipation, the consumption is proportional to the number of the used transistors. For dynamic power dissipation, the consumption is provided from the charging and discharging of load capacitance. The average dynamic dissipation of a CMOS gate is

$$P\ avg = \tfrac{1}{2}\ CfV_{dd}N$$

Where C is the load capacitance, f is the clock frequency, VDD is the power supply voltage and N is the number of switching activity in a clock cycle. Hence, it is very important for modern DSP circuit application to develop low-power multipliers to minimum the power dissipation.

In this paper we present a novel technique of multiplication that will serve our two important needs i.e. low power consumption and low area to make our design greener and compact.

III. Array Multiplication

In array multiplier, each partial product is generated by taking into account the multiplicand and one bit of multiplier each time. The Impending addition is carried out by high-speed carry-save algorithm and the final product is obtained by employing fast adder – the number of partial products depends upon the number of multiplier bits. A 4x4 array multiplier is shown in Figure 3. The structure of the full adder can be realized on FPGA. Each products can be generated in parallel with the AND gates. Each partial product can be added with the sum of partial product which has previously produced by using the row of adders. The carry out will be shifted one bit to the left and then it will be added to the sum which is generated by the first adder and the newly generated partial product. The shifting would carry out with the help of Carry Save Adder (CSA) and the

Ripple carry adder or any fast adder can be used for the final stage. [10].

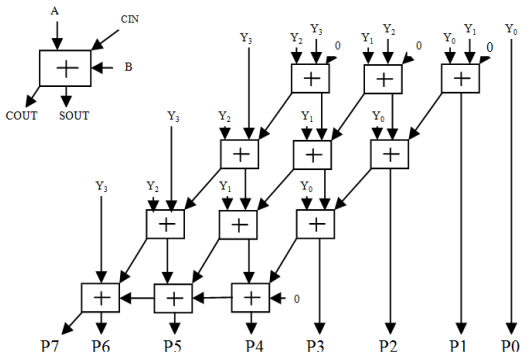

Figure 3: Array Multiplier

IV. HARDWARE EFFICIENT MULTIPLIER

In section III we have discussed simple array multiplier, we need to cut down the area requirement of the multiplier, there are many possibilities one of them is using low power adder. In this design we have reduced the number the layers in array multiplication method by reusing the middle layer again and again. Also we have used low power adders in these layers to further reduce the power consumption.

First we will discuss the different adders used in our design. In total 6 different adders are used to implement the design.

Simple full adder: The first adder we are using is the full adder. The logic diagram is shown in figure.

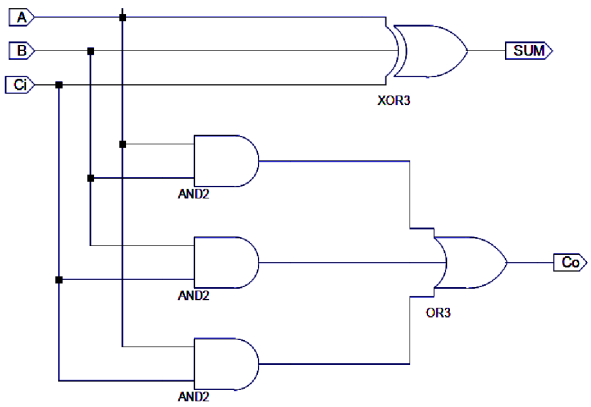

Figure 4: Simple Full Adder

Half Adder: The second adder is the simple half adder with two inputs and two outputs.

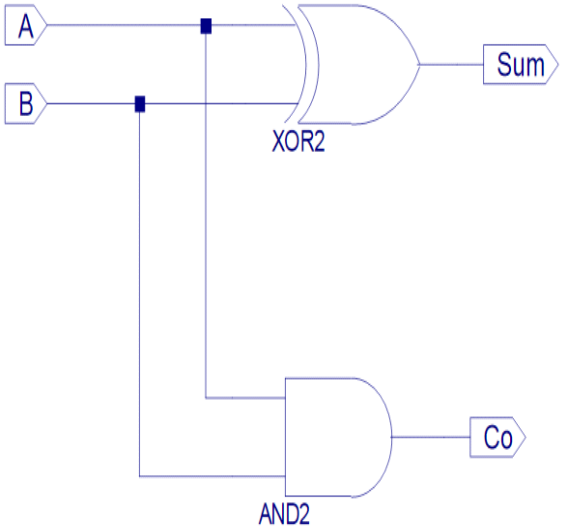

Figure 5: Half Adder

Row Column Adder Type – 1: This is the third adder we have in our design. This is the custom adder we have used with four inputs and two outputs. This is also a low power adder.

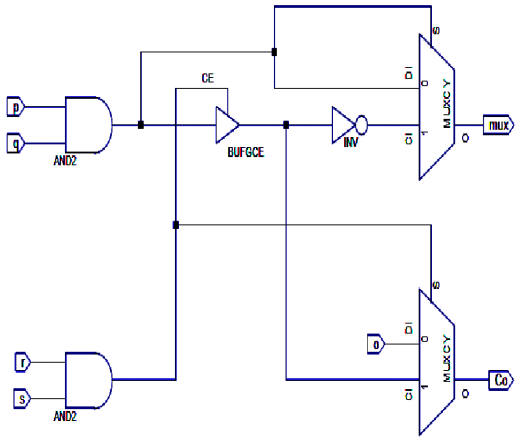

Figure 6: Row Column Adder Type – 1

Row Column adder type – 2: This is the fourth adder we have used in our design; this is again a custom adder for this design only. The adder has four inputs and two outputs. This is also a low power adder which tri-states the XNOR gate and OR gate under certain conditions.

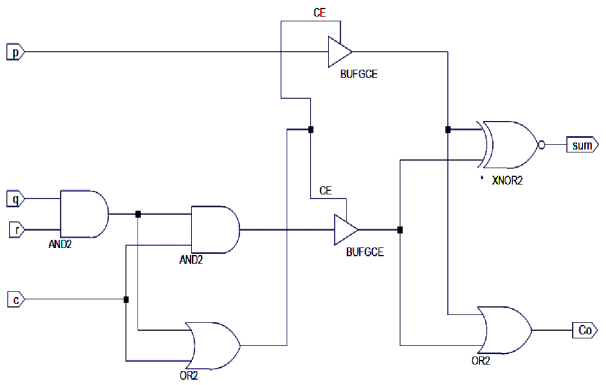

Figure 7: Row Column Adder Type – 2

Row Column Adder Type – 3: This is gain a custom adder we have used in this design. The adder has five inputs and three outputs in it. Multiplexers are employed to implement this adder.

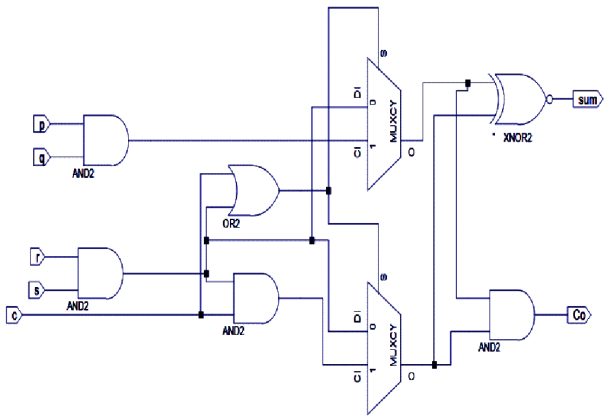

Figure 8: Row Column Adder Type – 3

In simple array multiplier as the number of bits for multiplication increases the resource requirement also increases. Half adder and full adder are the basic units for multiplier circuit and as the size of the multiplier increases the number of half adders and full adders also increases. So a large number of adders are required.

In array multiplication technique n rows of adder circuit is required for n x n multiplication. In this design first we have reduced the number of layers in array multiplier to only three. To implement this we have reused the middle layer of adders as shown in Figure 9. The partial products are generated and stored in flip flops and then stored results are used again for next level of partial products. The process is repeated till the end of multiplication. Since the number of adders in the design is reduced by a large amount the area requirement also reduces. The number of storage elements basically flips flops increases, but these elements are available in abundance in any FPGA and require less area. So the area requirement reduces.

The second level of optimization is the use of custom adders in the design. These adders type 1 through type 3 are special adders with less power consumption.

So our proposed design reduces the FPGA resource usage and power consumption of the design.

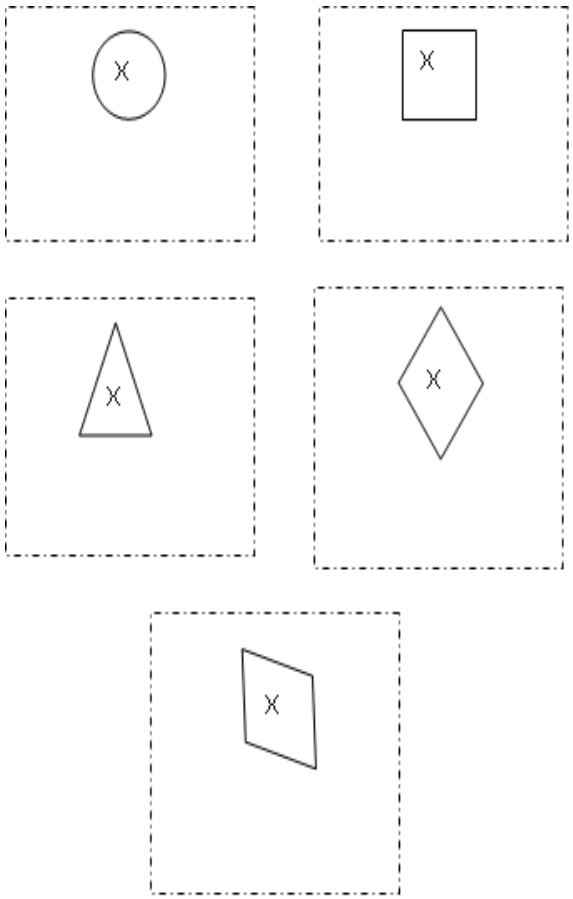

Figure 9: Representation of Different Adders

Figure 9 shows the different conventions used to represent different adders, and Figure 10 depicts the hardware efficient multiplier.

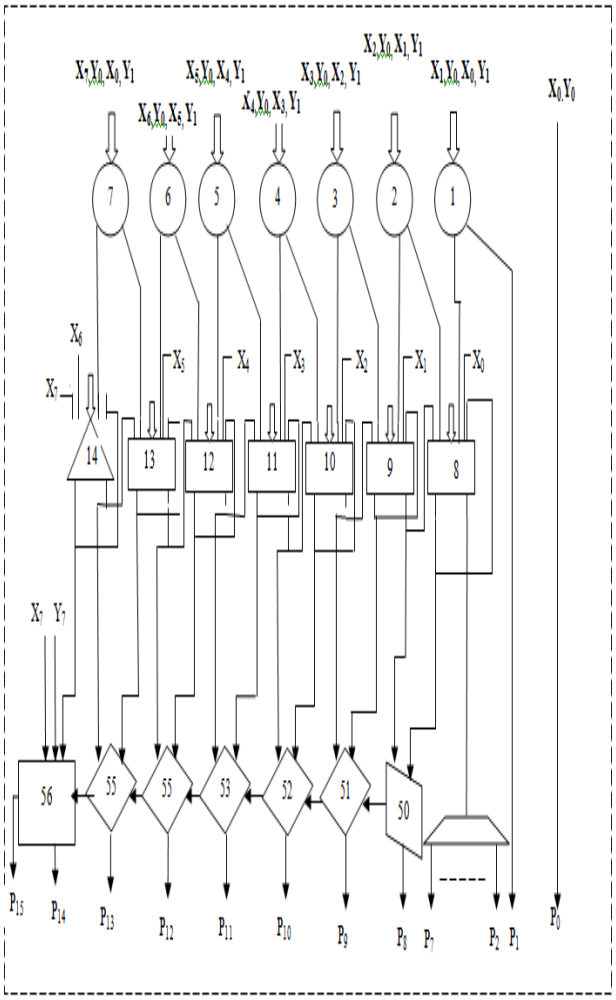

Figure 10: 8 x 8 Multiplier using hardware reuse method

V. RESULTS

In order to evaluate the performance of low power parallel multiplier, we implement all these designs on Spartan FPGA.

Table 1 shows the Cell Usage summary. And table 2 shows the device utilization summary. The 8 x 8 multiplier shown in figure 10 is regular in shape so, we have designed a 16 x 16 multiplier using same technique and here we have presented synthesis results.

Table 1: Cell Usage Summary (16 X 16 Multiplier)

Parameters (Cell Usage)	*Usage*
BELS	*189*
LUT2	*21*
LUT2_D	*1*
LUT3	*30*
LUT4	*133*
MUXF5	*4*
Flip Flops / Latches	*110*
FDCE	*3*
FDPE	*2*
LD	*106*
Clock Buffers	*3*
BUFG	*2*
BUFGP	*1*
IO Buffers	*66*
IBUF	*34*
OBUF	*32*

Table 2: Device utilization Summary (16 X 16 Multiplier)

Design	*Number of LUT's*
Without Bypassing[11]	*590*
Row Bypassed [11]	*921*
Proposed Design [11]	*941*
Our Design	*185*

Table 3 shows the power consumption of our design and we have also compared it with available multipliers in literature.

Table 3: Power Consumption report

Design	*Power Consumption*
Without Bypassing[11]	*44mW*
Row Bypassed [11]	*39mW*
Proposed Design [11]	*35mW*
Our Design	*30mW*

VI. CONCLUSION

We have implemented a hardware efficient multiplier on Spartan FPGA using only three layers of adders and few storage elements. We succeeded in curtailing the area requirement and the power consumption of the multiplier compared to previously available designs as seen from table 2 and table 3 respectively.

As we are using many storage elements (flip flops), clock gating can be used in future to further reduce the power consumption of the design.

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