Volume 4, Issue 1, January 2017 ISSN: 2348-8565 (Online)
International Journal of Modern Engineering and Research Technology
Website: http://www.ijmert.org Email: editor.ijmert@gmail.com

Design of Full Adder Using PTL & GDI Technique and Comparison with Conventional Designs

Nidhi Dubey
Research Scholar (M.Tech.)
Shri Ram Institute of Technology
Jabalpur (M.P.), [INDIA]
Email: niidhi.dubey25@gmail.com

Divyanshu Rao
Assistant Professor
Department of Electronics & Comm. Engineering
Shri Ram Institute of Technology
Jabalpur (M.P.), [INDIA]
Email:Divyanshu3@gmail.com

ABSTRACT

In this paper we have reviewed the used Pass transistor Logic and Gate diffusion Input technique to implement various Adder designs. Here we have implemented Adder using various designs so as to have less computation and less complexity. These Adder's at gate level can be designed using any technique such as CMOS, PTL only and TG but design with PTL and GDI technique combined gives better result in terms of area, switching delay and power dissipation. Different Adder designs are being implemented with PTL & GDI technique in DSCH 3.5 and layout generated in Microwind tool. The Simulation is done using 65 nm technology at 1.2 v supply voltage and result is compared with conventional CMOS technique. Simulation result shows great improvement in terms of area, switching delay and power dissipation.

Keywords:—*GDI, PTL, CMOS, Switching Delay, Power dissipation*

I. INTRODUCTION

Arithmetic circuits, like Adders and Subtractor, are one of the basic components in the design of Arithmetic and Logical Unit's. Designing low power high-speed arithmetic and logical Unit requires a combination of techniques at four levels; algorithm, architecture, circuit and system levels. This thesis presents layout and simulations of different ALU designs, which is suitable for high-performance and low–power applications. ALU is one of the most important components for any digital system, such as Central Processing Unit of Computers. Therefore a fast and precise operation of a digital system is greatly enhanced by the performance of the existing ALU designs. Adders are one of the most significant component in Arithmetic and Logic Unit because of their widespread application in digital operations such as addition, multiply and division. Hence, improving performance of the digital adder would greatly enhance the execution of binary operations inside ALU of Computer systems. The power dissipation in a ALU is a very important parameter as it reflects the total power dissipation of the system and hence drastically affects the performance of the device.

The rapid growth in market of electronic devices had boomed the IC engineers. Meanwhile, as the daily used portable IC devices, such as, mobile phones, laptop etc., VLSI engineers are working to improve the performance of existing operation modules in some aspects, especially in reducing the power consumption and size. Low power for devices can be achieved by selecting new technology or implementing a new logic. Technology

means scaling down the size of transistor, which further help in reducing the area and power. Second term is logic, which implies reducing power and area by changing the logic while keeping the transistor size constant. Reducing the size of transistor can be achieved by selecting the 180nm or 90 nm or 65nm or 45nm technology file but the basic challenge is when the technology file is constant and new logic should be implemented. PTL is one of the design techniques, which allows implementation of a wide range of complex logic functions using very less number of transistors. This method is suitable for design of fast, low power circuits, using a relatively less number of transistors (as compared to Conventional CMOS techniques), while improving logic level swing and static power dissipation and allowing simple top-down design by using small cell library Multiplexers and Full Adder are been designed using pass transistor logic and GDI technique. The pass transistor design reduces the parasitic capacitances and results in fast circuits.

In this paper, we have designed adder using PTL and GDI combined and reviewed our design with conventional CMOS design. Full Adder, has been implemented by CMOS and then by GDI & PTL technique in MICROWIND & DSCH tools with 65nm technology with 1.2v supply voltage. The W/L ratio of both nMOS and pMOS transistors are taken as 1.0/0.12ìm. To establish an unbiased testing environment, the simulation of ALU designs have been carried out using extensive input bits, which covers every possible transition for every input bits combinations.

II. CMOS Design Technique

There are numerous circuit styles to implement a given logic function. the common design metrics by which a logic design is evaluated include area, speed, energy and power. In addition to these metrics, robustness to noise is also a very important consideration. Recently, power dissipation has also become a very important requirement and significant emphasis is placed on understanding the sources of power and approaches to deal with power.

The most widely used logic style is static complementary CMOS. The static CMOS style is really an extension of the static CMOS inverter to multiple inputs. The primary advantage of the CMOS structure is robustness (i.e., low sensitivity to noise), good performance, and low power consumption (with no static power consumption). The complementary CMOS circuit style falls under a broad class of logic circuits called static circuits in which at every point in time (except during the switching transients), each gate output is connected to either V_{DD} or V_{ss} via a low-resistance path.

A static CMOS gate is a combination of two networks, called the pull-up network (PUN) and the pull-down network (PDN) (Figure 4.8). The figure shows a generic N input logic gate where all inputs are distributed to both the pull-up and pull-down networks. The function of the PUN is to provide a connection between the output and VDD anytime the output of the logic gate is meant to be 1 (based on the inputs). Similarly, the function of the PDN is to connect the output to VSS when the output of the logic gate is meant to be 0. The PUN and PDN networks are constructed in a mutually exclusive fashion such that one and only one of the networks is conducting in steady state. In this way, once the transients have settled, a path always exists between VDD and the output F, realizing a high output (“one”), or, alternatively, between VSS and F for a low output (“zero”). This is equivalent to stating that the output node is always a low-impedance node in steady state.

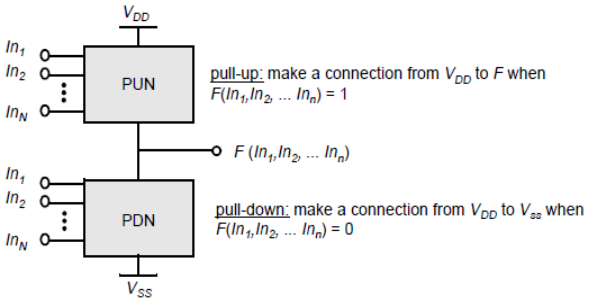

Figure 1 Complementary logic gate with PUN & PDN

III. PTL & GDI Technique

Pass Transistor Logic

A popular and widely used alternative to complementary CMOS is pass transistor logic. Pass transistor logic attempts to reduce the number of transistors required to implement logic by allowing the primary inputs to drive gate terminals as well as source/drain terminals. Figure 4.9 shows a transistor level implementation of the AND function constructed using NMOS transistors. In this gate, if the B input is high, the top transistor is turned on and copies the input A to the output F. When input B is low, the bottom pass transistor is turned on and passes a 0. The switch driven by B seems to be redundant at first glance. Its presence is essential to ensure that a low-impedance path exists to the supply rails under all circumstances.

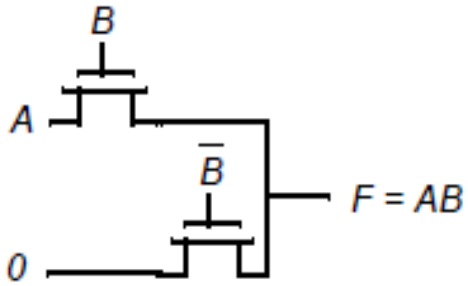

Figure 2 Pass-transistor implementation of an AND gate

The potential advantage of pass transistor is that a fewer number of transistors are required to implement a given function. For example, the implementation of the AND gate in Figure2 requires 4 transistors (including the inverter required to invert B) while a complementary CMOS implementation would require 6 transistors. Pass transistor logic uses fewer devices and therefore has lower physical capacitance. Unfortunately a NMOS device is effective at passing 0 but is poor at pulling a node to V_{DD}.

Gate Diffusion Input Technique

The GDI technique offers realization of extensive variety of logic functions using simple two transistor based circuit arrangement. This scheme is appropriate for fast and low power circuit design, which reduces number of MOS transistors as compared to CMOS and other existing low power techniques, while the logic level swing and static power dissipation improves. It also allows easy top-down approach by means of small cell library The basic cell of GDI is shown in Figure 3

1. The GDI cell consists of one nMOS and one pMOS. The structure looks like a CMOS inverter. Though in case of GDI both the sources and corresponding substrate terminals of transistors are not connected with supply and it can be randomly biased.

2. It has three input terminals: G (nMOS and pMOS shorted gate input), P (pMOS source input), and N (nMOS source input). The output is taken from Out (nMOS and pMOS shorted drain terminal)

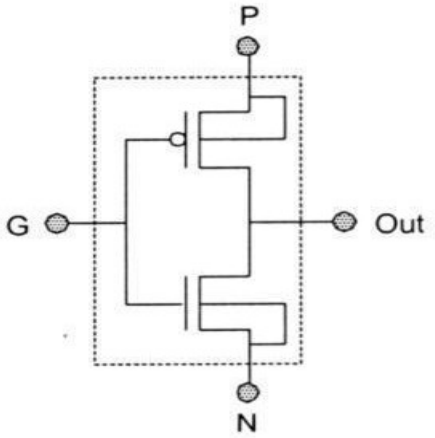

Figure 3 Basic GDI cell

GDI logic style approach consumes less silicon area compared to other logic styles as it consists of less transistor count. In view of the fact that, the area is less, the value of node capacitances will be less and for this reason GDI gates have faster operation which presents that GDI logic style is a power efficient method of design.

IV. Implementation of Adder Using CMOS Technique

Full Adder is the one of the basic element in Digital Circuits. It is also one of the critical building blocks of the multiplier. We can deduce the Boolean function in SOP form for full adder as the following:

Here A and B are the inputs to the adder, C is the input carry, SUM is the output for add operation, and CARRY is the output for any carry generated. The generate signal, G, is high only when a carry output (CARRY) is internally triggered within the adder. When the propagate signal, P, is high, the carry-in signal C is passed on to the carry output CARRY. Because the Carry-in status of the current bit is obtained by lower of two operand bits, the delay of the adder therefore depends on the carry generation.

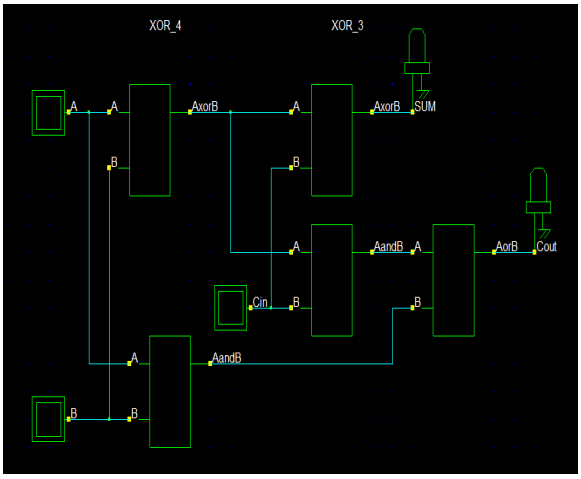

Figure 4 CMOS Full Adder Using Gates

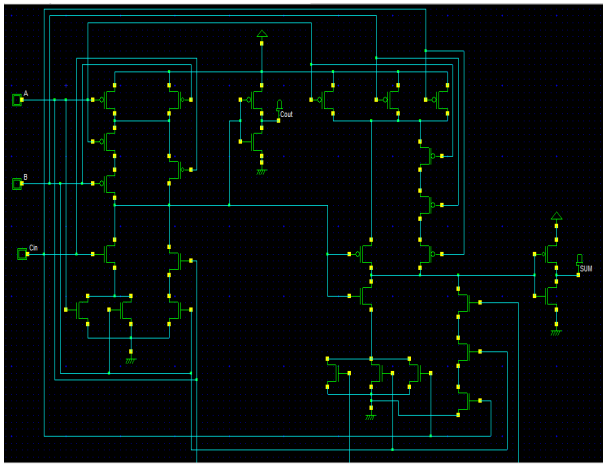

Figure 5 CMOS Full Adder Using 28 Transistors

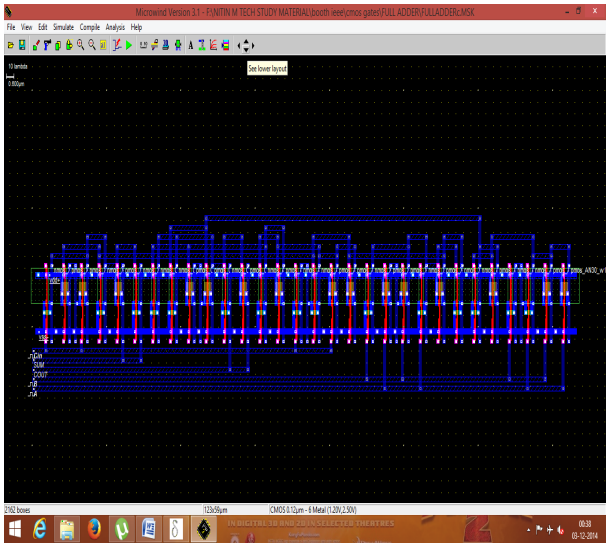

Figure 6 Layout of CMOS Full Adder Using Gates

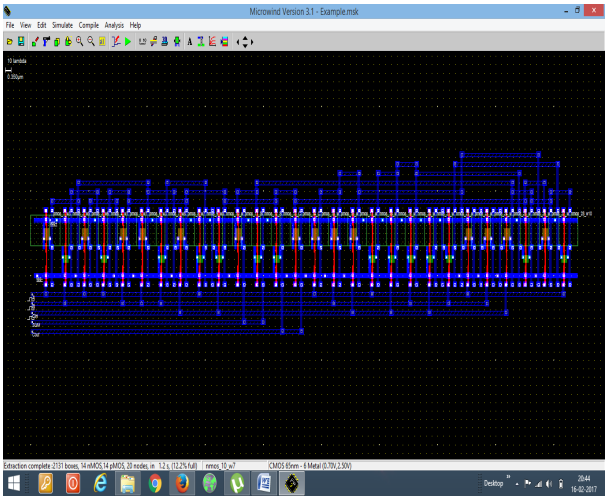

Figure 7 Layout of CMOS Full Adder Using 28 Transistors

V. Implementation of Adder Using PTL and GDI Technique

Full Adder can also be implemented using combined technique (GDI & PTL). This Full Adder design can also be reconfigured to be used as AND,OR,XOR and INVERTER gate along with addition operation. The modified equations for Full adder for this purpose are as follows:

$$sum = (a \oplus b) \oplus c$$
$$=> (a \oplus b)c`+(a \oplus b)`c$$
$$carry = ab + bc + ca$$
$$=> (a \oplus b)`a + (a \oplus b)c$$

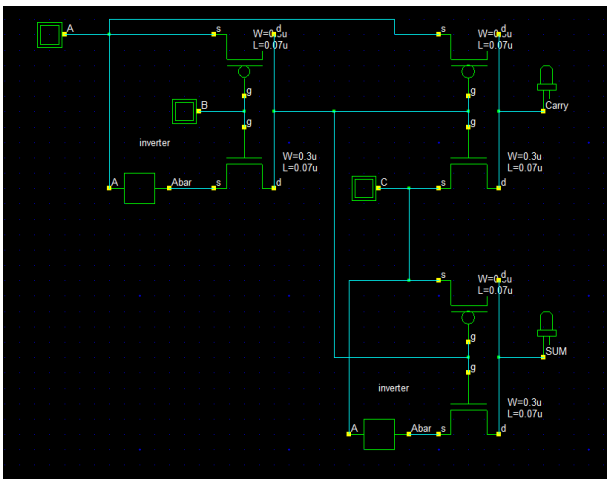

Figure 8 PTL & GDI Based Adder

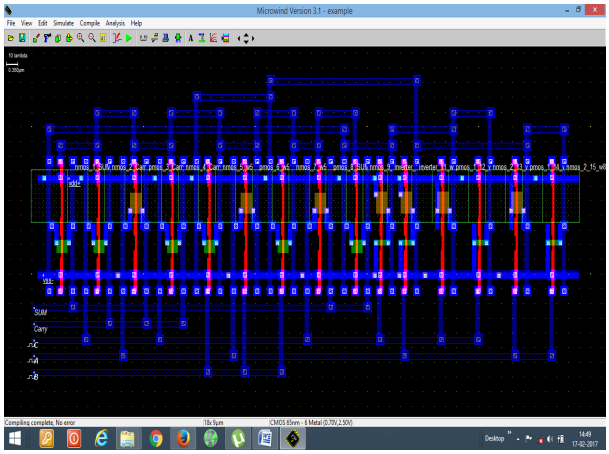

Figure 9 Layout of PTL & GDI Based Adder

Table 1 PTL Adder Analysis

S.NO.	PARAMETERS	VALUE
1	SWITCHING DELAY (ns)	0.32
2	VERILOG FILE SIZE (Lines)	35
3	POWER DISSIPATION	20
4	COMPILED CELLS	15
5	ROUTED WIRES	36
6	NO. OF NMOS TRANS. USED	3
7	NO. OF PMOS TRANS. USED	3
8	ELECTRICAL NODES COMPILED	11
9	AREA (μ m²)	123.3
10	TRANSISTORS USED	6
11	POWER DISSIPATION (μW)	16.306

Table 2 CMOS Adder Analysis

S.NO.	PARAMETERS	VALUE
1	SWITCHING DELAY (ns)	0.61
2	VERILOG FILE SIZE (Lines)	49
3	POWER DISSIPATION	39
4	COMPILED CELLS	28
5	ROUTED WIRES	56
6	NO. OF NMOS TRANS. USED	14
7	NO. OF PMOS TRANS. USED	14
8	ELECTRICAL NODES COMPILED	20
9	AREA (μ m²)	249.3
10	TRANSISTORS USED	28
11	POWER DISSIPATION (μW)	25.146

VI. Conclusion

This paper has presented the architecture design, logic design and circuit implementation of Single Bit Full adder. The objective for Area, delay and power in Multipliers was carried out for bit addition using CMOS and PTL & GDI techniques and Comparison with CMOS Technique are shown in Table 1 & 2.

The Adder designed with PTL & GDI technique gives less delay and less power dissipation with higher-speed of operation as compared to CMOS Technique.

VII. ACKNOWLEDGMENT

I would like to say thanks to my guide Asst. Prof. Mr. Divyanshu Rao who gave their knowledge and time in order to complete this paper. This paper will never complete without the support faculty member of ECE department of S.R.I.T College, Jabalpur.

REFERENCES:

[1] G.Karthik Reddy "*Low Power-Area Pass Transistor Logic Based Alu Design Using Low Power Full Adder Design*" IEEE 2015.

[2] K. Nehru, A. Shanmugam. Dr.G. Darmila Thenmozhi "*Design Of Low Power Alu Using 8t Fa And Ptl Based Mux Circuits*" IEEE March 2012.

[3] G.Saranya, S.Kiruthika, "*Optimized Design Of An Alu Block Using Architectural Level Power Optimization Techniques*" IEEE November 2015.

[4] Karthik Reddy.G, "*Low Power-Area Designs Of 1bit Full Adder In Cadence Virtuoso Platform*" 2013.

[5] Yi Wei, Ji-Zhong Shen "*Design Of A Novel Low Power 8-Transistor 1-Bit Full Adder Cell*" JZHU July 2011.

* * * * *