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A Novel Approach for Arithmetic Execution Unit for High Speed Application

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ABSTRACT

This paper presents Multiply and Accumulate (MAC) unit design using Vedic Multiplier, which is based on Urdhva Tiryagbhyam Sutra. The paper emphasizes an efficient 32-bit MAC architecture along with 8-bit and 16-bit versions and results are presented in comparison with conventional architectures. The efficiency in terms of area and speed of proposed MAC unit architecture is observed through reduced area, low critical delay and low hardware complexity. The proposed MAC unit reduces the area by reducing the number of multiplication and addition in the multiplier unit. Increase in the speed of operation is achieved by the hierarchical nature of the Vedic multiplier unit. The performance evolution results in terms of speed and device utilization are compared to earlier MAC architecture.

Keywords:—*Vedic Multiplier AEU, FPGA, Xilinx-ISE 14.1 .*

I. INTRODUCTION

The general MAC architecture consists of a conventional multiplier, adder and an accumulator. Where the output is added to the previous MAC output result by an accumulate adder. The Multiply-Accumulate (MAC) unit is extensively used in microprocessors and digital signal processors for data-intensive applications, such as filtering, convolution, and inner products. Most digital signal processing methods use nonlinear functions such as discrete cosine transform (DCT) or discrete wavelet transform (DWT) or FFT/IFFT computations that can be efficiently accelerated by dedicated MAC units. Because they are basically accomplished by repetitive application of multiplication and addition, the speed of the multiplication and addition determines the execution speed and performance of the entire computation. As the multiplier exhibits inherently long delay among the basic operational blocks in digital system, the multiplier determines the critical path. In order to improve the speed of the MAC unit, there are two major bottlenecks. The first is the partial products reduction network that is used in the multiplication block and the second is the accumulator. Both of these stages require addition of large operands that involve long paths for carry propagation. The main key to the proposed architecture is using the Vedic multiplier to design the MAC unit and compare the performance with the conventional MAC units in terms of area, speed and number of resources.

In computing, especially digital signal processing, most common operation is which get performed is arithmetic operation.

The AEU unit shown in the block diagram is able to perform arithmetic operations such as Addition, Subtraction, Multiplication, Squaring and comparison operations. Furthermore arithmetic operations are also very important and dominant for digital filters.

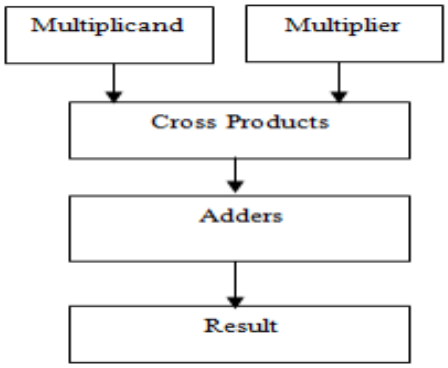

Figure 1: Architecture of Vedic Multiplier.

II. Proposed AEU Unit

Proposed Multiplication Unit design:-

Multiplication Accumulation is an important part of real-time digital signal processing (DSP) with applications ranging from digital filtering to image processing. Multiply and accumulate is a very common basic-level operation seen in many DSP designs/algorithms. Two numbers are multiplied together, and added into an accumulator register. As shown in Fig.4, the basic MAC unit consists of multiplier, adder and accumulator. In general MAC unit uses the conventional multiplier unit, which consists of multiplication of multiplier and multiplicand based on adding the generated partial products and to compute the final multiplication. This results to adding the partial products. The key to the proposed MAC unit is to enhance the performance of MAC using Vedic Multiplier and to compare the Vedic, Booth and conventional multiplier in terms of computation required to generate the partial products and add the generated partial products to get the final result of the multiplication For 2 bit level we have proposed to use conventional Vedic multiplier, whose digital hardware is shown below:-

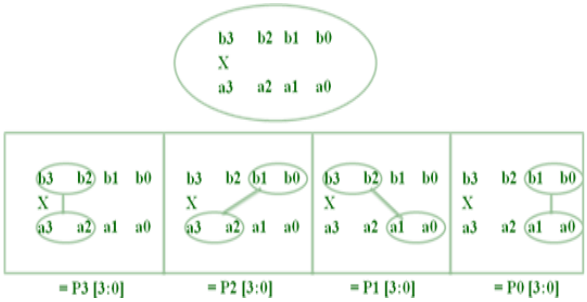

Figure 2 : Proposed Four Bit Vedic Multiplier Using Divide And Conquer Approach

In the above diagram the oval shape represents multiplier and multiplicand respectively. And the line between these oval shapes represents that multiplication operation being occurred. It can be seen from above given diagram that to multiply four-bit numbers say b [3:0] and a [3:0], four sub-multiplication operations need to be performed, using the two bit Vedic multiplier. Means to perform the four-bit multiplication, the two-bit multiplier has been instantiated four times. Then the addition tree structure has been used to add these partially generated product outputs of two-bit multiplier. As shown in the following:-

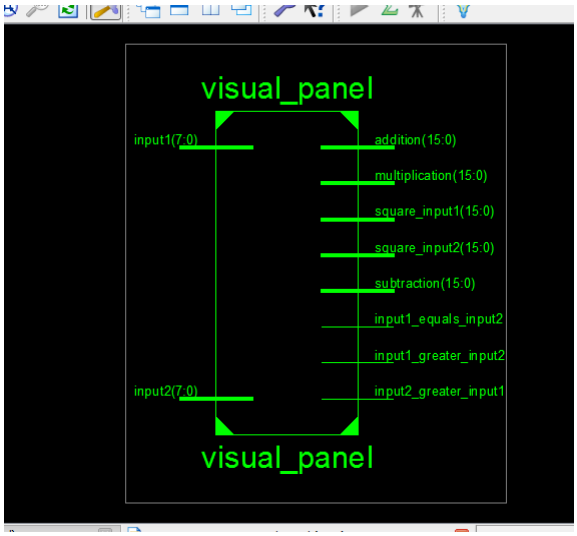

Figure 3: Top View of AEU

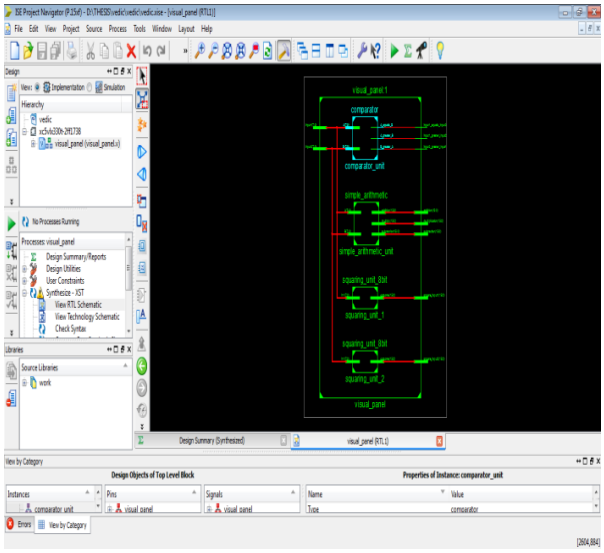

Figure 4: RTL view of AEU

III. Simulation and Synthesis Result

1. Platform being used: - For this design the target FPGA, which has been used belongs to Spartan-2 (family), XC2S200 (device), PQ208 (package) with speed grade of -6. Xilinx synthesis tool (XST) of Xilinx ISE-14.1 has been used for synthesis purpose. For the behavioural simulation purpose ISE simulator has been used.

Property Name	Value
Product Category	General Purpose
Family	Spartan2
Device	XC2S200
Package	PQ208
Speed	-6
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISE Simulator (VHDL/Verilog)
Preferred Language	Verilog
Enable Enhanced Design Summary	☑
Enable Message Filtering	☐

Figure 5: Target FPGA for our module

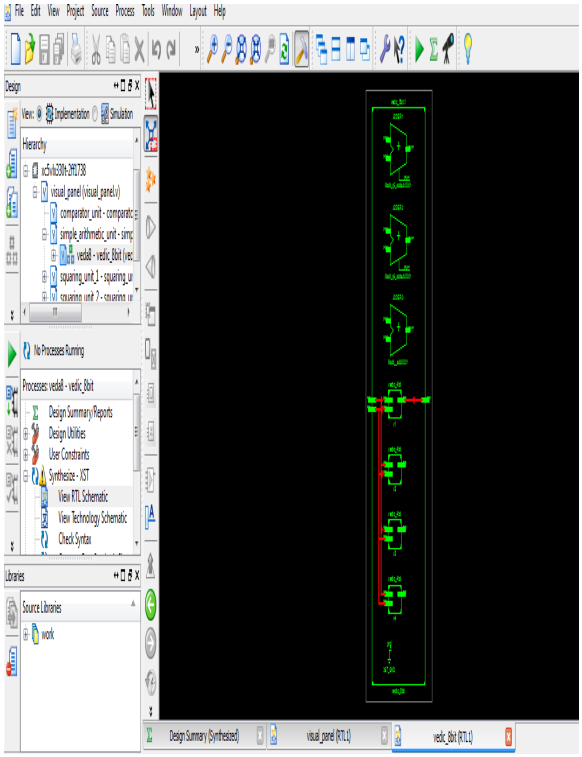

Figure 6. 8-Bit Vedic Multiplier RTL Schematic

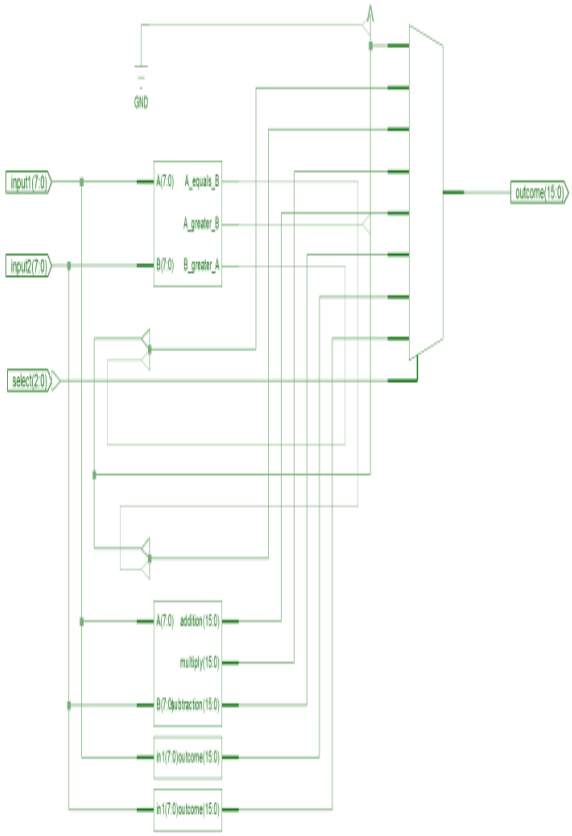

Figure 7 : Proposed 8 Bit Single Visual Panel RTL Schematic

2. Device Utilization Summary:-

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	376	4,704	7%	
Logic Distribution				
Number of occupied Slices	211	2,352	8%	
Number of Slices containing only related logic	211	211	100%	
Number of Slices containing unrelated logic	0	211	0%	
Total Number of 4 input LUTs	411	4,704	8%	
Number used as logic	376			
Number used as a route-thru	35			
Number of bonded IOBs	35	140	25%	
Total equivalent gate count for design	3,345			
Additional JTAG gate count for IOBs	1,680			

Figure 8: Device Utilization Summary of Proposed 8-Bit Arithmetic Execution Unit

Simulation Results:-

Proposed 8-bit Arithmetic Execution Unit simulation waveform, where inputs and output are in decimal format: -

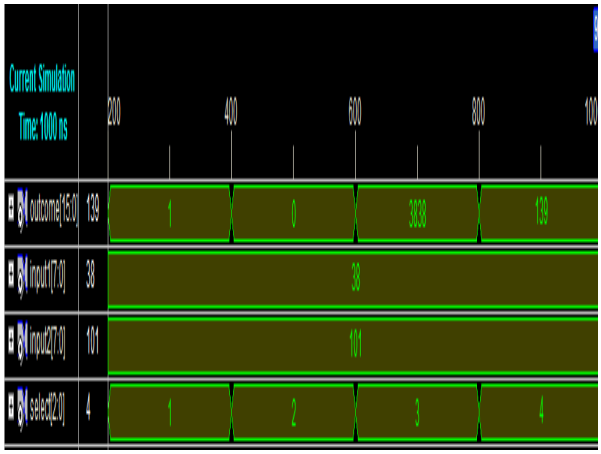

Figure 9: Proposed 8-Bit AEU Unit Simulation Waveform

IV. COMPARATIVE RESULTS

Proposed Arithmetic Execution Unit (AEU)'s speed solely depends upon effectiveness and efficiency of proposed Vedic multiplier. That's why to showcase efficiency and effectiveness of proposed Vedic multiplier that has been implemented and compared with other popular commercially available multiplication structures lie on different multiplication algorithms on the same platform of target FPGA, which has been used to implement these popular multiplier structures. Proposed module has been compared against different modules with same target FPGA on which previous has been implemented and then showcased comparison on the basis of availability of results. Comparison tables are shown below:-

Table 1: Comparison Modules with Same Target FPGA

Parameters	Vishal Galphat, Nitin Lonbale [1]	Result Obtained
No. of slice LUTs	17	14
No. of bonded IOBs	18	16
Propagation Delay (ns)	7.881	7.858

V. CONCLUSION

In this research work a thorough analysis and study work has been done on Vedic multipliers and we have found that Vedic with CSA provides much better outcome than commercially available multipliers likewise Booth, Wallace, Modified Booth Wallace multipliers etc. So we have used this multiplier to perform all multiplication operations being used in various operations of Arithmetic Execution Unit those are square and multiplication unit. After synthesis and simulation work for proper validations has been performed on this AEU to have reliability on our proposed designed module.

VI. APPLICATION

Arithmetic Execution Unit performed operations are very important and dominant for digital filters. Therefore, by the use of speed optimized AEU high-speed filtering can be achieved.

AEU is also useful to optimize other processing typical for DSP applications.

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