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The Design of Low Power CMOS based Booth Multiplier

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ABSTRACT

The demand of high speed and low power processors are increasing nowadays due to advancement in technology. The multipliers play a crucial role for the processors because the speed of multipliers affect the allover speed of processors as many operation like shifting is carried by the help of multipliers. The booth multiplier is a multiplier which is used in many practical devices especially in the field of digital image processing and FIR filters. Booth multiplier works on algorithm which is booth algorithm. The main advantage of booth algorithm is that it converts the multiplicand bit into booth equivalent bit which help in reduction of chip size of the multiplier by reducing the required partial product into the half. Beside from non-volatile behavior of memory it offers many applications in a field of neural networks, robotics, low power sensors and analog computation. This paper introduced implementation of low power booth multiplier booth multiplier by the help of CMOS logic. The result obtained is in form of average power and noise at 45nm technology. The input voltage for the circuit is varies from 0.5 to 0.7 volt.

Keywords:— *CMOS, Booth Multiplier, Cadence Virtuoso and Logic Gates.*

I. INTRODUCTION

Due to the advancement in technology especially in the field of VLSI, the demand of high speed power electronic devices is rapidly increasing. So many researchers tried to propose a design which can offers less leakage power and noise. Also the chip size of the circuit reduces due to which delay time of the circuit is also reduces. In today world the demand of portable and batter power devices like mobile phones, PDA tools and laptops is continuously keep on increasing due to the advancement of technology. So the need of low powered devices is becomes a major topic of concern. The power consumption in the circuit also affects the battery life of the devices. There are several techniques that used in the reduction of leakage of current and voltage also allow less power consumption. Out of which CMOS is the basic technique because it is very easy to fabricate but the number of transistor used in CMOS in more.

II. CMOS LOGIC

Both N-type and P-type transistors are used in CMOS logic style to design logic functions. When matching signal is given to CMOS it turned on one transistor and turn off another transistor.

In CMOS logic gates n-type MOSFETs are sand witched between the lower voltage power supply rail and output and it is used in a

pull down network and p-type MOSFETs are used in a pull up network sand witched between the output and the higher voltage rail. Both p-type and n-type transistors are joined to the identical input, one type of the MOSFET will be on immediately as other MOSFET is off, and vice-versa.

Due to more number of transistors its transistor count is increases and its power consumption also increases. As the technology reduce circuit works on less power, as a result this design is not very useful in today's modern era. Problem of voltage scaling and transistor sizing is not more in CMOS circuits. Noise margin in CMOS circuits is high and low voltage is given to the circuit. Connection of input signals to gates of transistor only, gives the advantage of usage and categorization of logic cells. The complementary transistor pair makes the layout of CMOS gates efficient and straight forward.

III. BOOTH MULTIPLIER

Booth multiplier is a type of digital multiplier. The first booth multiplier was simulated by Andrew Donald in 1951. The booth algorithm helps to multiply the signed bits. The booth multiplier is mainly used in a field of digital signal processing and FIR filter as it performs some of the basic operation like filtering and convolution. Booth multiplier is mainly used for the application where there is a need of very high speed as it cuts the required partial product into half which increases the speed of the multiplier. As most of the power consumption and delay arises due to the power partial product only. So the booth first converts the input multiplicand value to the both equivalent value. The three sections of booth multiplier are booth decoder, partial generating unit, half adder and full adder.

Booth Decoder

The working of decoder is to convert the input multiplicand value to the equivalent value. Because the equivalent value consists of more number of zero's hence it reduces the number of partial product as compared to the 2's complement value of input. The below figure consists of a diagram of booth decoder.

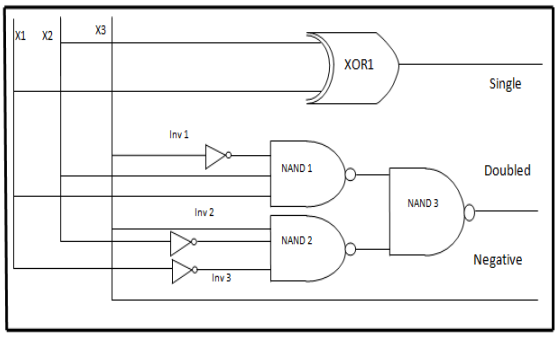

Figure 1- Booth Decoder circuit diagram

The above figure represents a circuit diagram of booth multiplier using CMOS logic gates. There are mainly 3 logic gates used in the implementation of booth decoder that are Inverter or a NOT gate, NAND gate and XOR gate. Here two inputs bits is passed to the decoder and the output is in the form of single, double and negative bit.

Partial Generating Unit

In this block the multiplicand bit is multiplied with the output of decoder unit to form a partial product output. Here the equivalent value is converted to the single bit partial product which is later provided to the adder circuit to generate the output of booth multiplier. The circuit diagram of partial generating unit is given below.

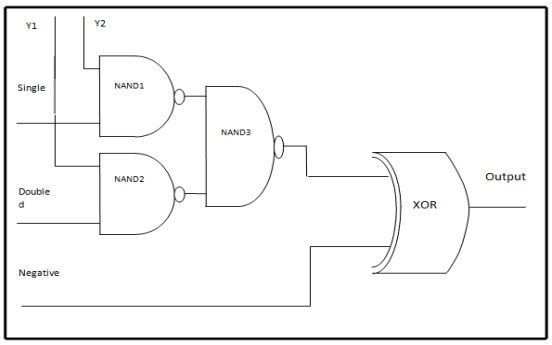

Figure 2: Partial Generating Unit Circuit Diagram

IV. Result and Simulation

In this chapter the implementations and simulation of CMOS technique is take place. The simulation is performed with the help of software CADENSE VIRTUOSO at 45nm. The result calculated is in the term of average power and noise. The input value is taken to the 0.7V. Here the simulated waveform show that the switching activity in CMOS technique is more as compared to GDI technique which give rise to the static and dynamic power dissipation in the circuit.

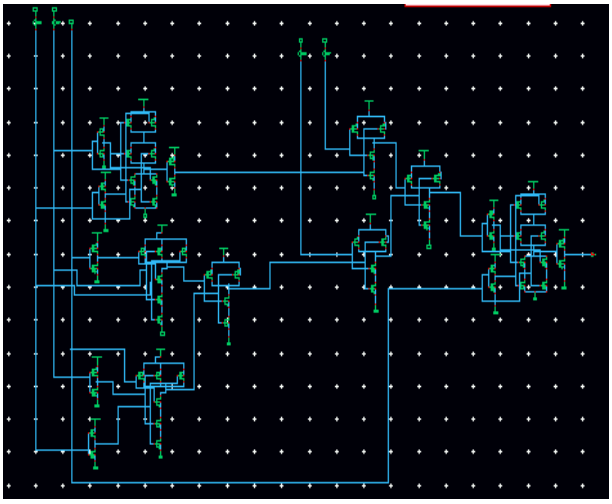

Figure 3. CMOS Implementation of Booth Multiplier

The below figure contain the simulated waveform of the booth multiplier using CMOS technique.

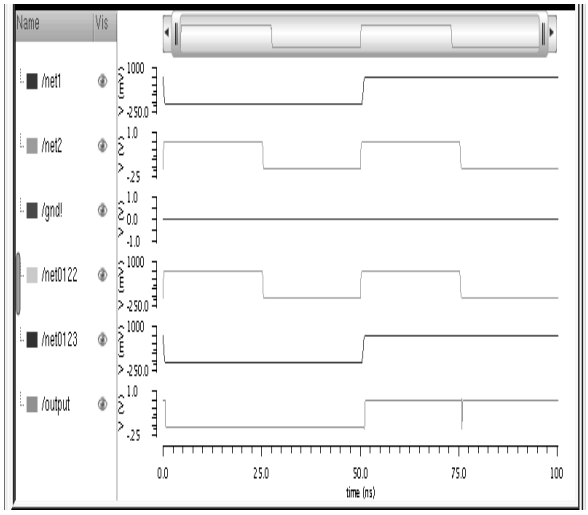

Figure 4. Simulated CMOS Booth Multiplier Waveform

Table 1: Average Power and Noise in CMOS booth multiplier

Input Value	Power (µW)	Time Delay (ns)
0.5	599.06 e^{-6}	205.817 e^{-15}
0.6	602.03 e^{-6}	205.817 e^{-15}
0.7	615.57 e^{-6}	205.817 e^{-15}

From above truth table it is shown that with the reduction of booth multiplier input power the average power consumption is reduces. But as the earlier told with the reduction of power to a very extent the noise is also start to increases.

V. Conclusion

In this paper a modified booth multiplier implemented using CMOS technique in 45 nm using a tool cadence virtuoso. With the help of output value we conclude that with the increase in input value the noise in the circuit is increases with it because as seen in table as value increases from 0.5 to the 0.7 the value of the Power reduces. And the time delay start increases but with a very less value with the increase in the value of the input.

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