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An Efficient Implementation of Zigbee Transmitter on FPGA Using Verilog

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ABSTRACT

The past several years have witnessed a rapid development in the wireless network area. So far wireless networking has been focused on high-speed and long range applications. Zigbee technology was developed for a Wireless Personal Area Networks (WPAN), aimed at control and military applications with low data rate and low power consumption. Zigbee is a standard defines the set of communication protocols for low-data-rate short-range wireless networking. Zigbee-based wireless devices operate in 868 MHz, 915 MHz, and 2.4 GHz frequency bands.

Keywords:— *Zigbee, WPAN, VHDL, MAC*

1. INTRODUCTION

Zigbee is a low data rate, low power, and low cost wireless networking protocol based on the IEEE 802.15.4, which is a set of new communication protocols for wireless transmission. Zigbee protocol defines the media access control (MAC) and physical (PHY) layers for low rate WPANs. It supports the frequency bands 868 MHz for European countries, 915 MHz for the United States, and 2.4 GHz for worldwide.

Main network topologies used in ZigBee wireless networking are star and peer-to-peer networks. In the star topology, every device in the network can communicate only with the personal area network coordinator. A Full Function Device takes up a role as PAN coordinator; the other nodes can be Reduced Function Device or Function Device. In the peer-to-peer topology, each device can communicate directly with any other device if the devices are close enough together to establish a successful communication link. Any Function Device in this topology can play the role of the personal area network coordinator.

Zigbee digital transmitter in 2.4GHz band is designed using VHDL for acknowledgement frame. MAC frame structures consist of beacon, data, acknowledgment, and MAC command frames. The MAC layer defines two types of nodes: Reduced Function Devices and Full Function Devices. The beacon frame is used by a coordinator to transmit beacons.

The function of beacons is to synchronize the clock of all the devices within the same network. The data frame is used to transmit data. Meanwhile, the acknowledgement frame is used to confirm successful frame reception. The Zigbee digital transmitter is designed for acknowledgment frame which is shown in Figure 1 based on IEEE 802.15.4 Standard.

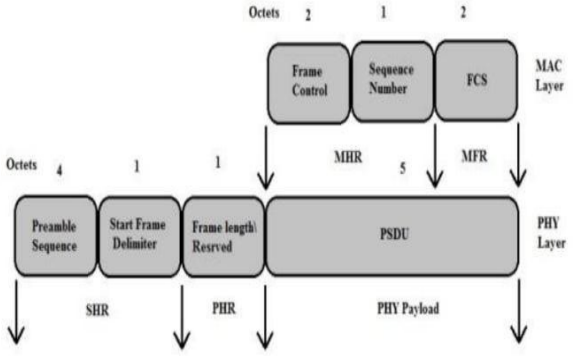

Figure 1. The Acknowledgment Frame

The acknowledge frame used contains 11 octets (i.e. 88 bits) of physical protocol data unit (PPDU). The binary data from the PPDU packet are inserted into the cyclic redundancy check block to detect errors during transmission. The Cyclic Redundancy Check is the most powerful of the redundancy checking techniques, the CRC is based on binary division. In CRC a sequence of redundant bits, called the CRC or the CRC remainder is appended to the end of a data stream. The resulting data becomes exactly divisible by a second, predetermined binary number. At its destination, the incoming data is divided by the same number. The diagram below will show you the Sequence of Events that takes place when using CRC. CRC's can detect all one bits and two bits errors as well as all odd number of bits in error. Since CRC is a technique for detecting errors, but not for making corrections when errors are detected, the whole packet data will be retransmitted if error occurs. For Zigbee Standard, CRC involves a division of the transmitted packet data by a constant called the generator polynomial. The CRC block contains the SHR, PHR and PHY payload. In the PHY payload, the FCS mechanism employs a 16-bit CRC in order to detect errors. The FCS is calculated over the MHR and MFR payload parts of the frame using the algorithm Every four bits of PPDU octet are mapped onto one data symbol, which will take place in bit-to -symbol block. The symbol block will be spread into 32-chip PN sequence by utilizing Direct Sequence Spread Spectrum method in Symbol-to-chip block. Then, the chips will be modulated using OQPSK technique.

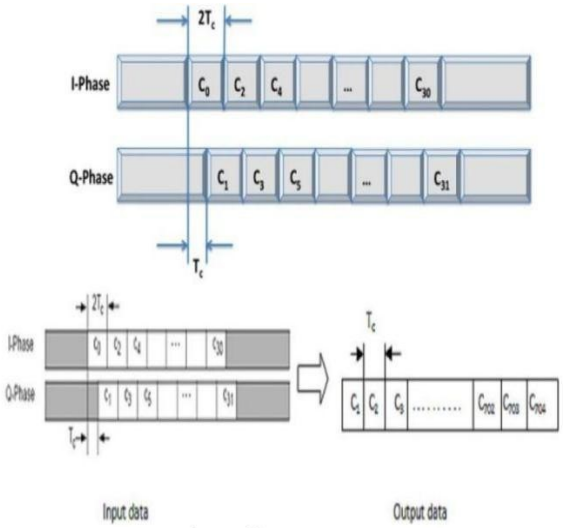

Figure 2: OQPSK chip offsets

frames which is originated from MAC sub-layer is inserted into the CRC block. Then, every 4 bits are mapped into one data symbol in the bit-to-symbol block. After that, these chips are processed by OQPSK (Offset Quadrature Phase Shift Keyed) modulator.

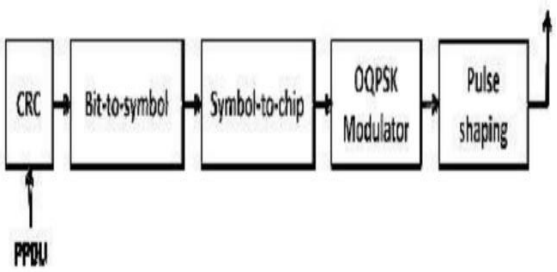

Figure 3: Transmitter block

OQPSK (offset QPSK) is a special version of QPSK in which the transmitted signal has no amplitude modulation. This disadvantage of a amplitude modulation are a result of 180° shifting in the phase. In OQPSK the incoming signal is divided in the modulator into two portions I and Q which are then transmitted shifted by a half symbol duration. The phase plane of a OQPSK is shown in Figure 3. There is no phase shift through the zero crossing which means there are no phase shifts by 180° as in a standard QPSK.

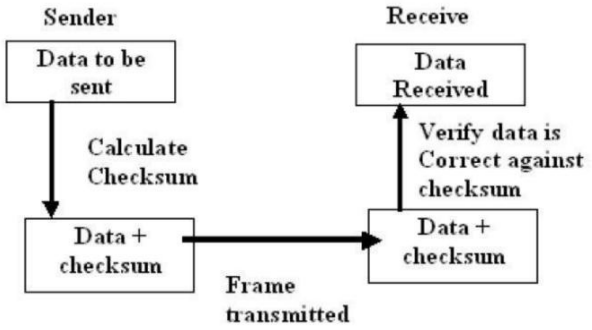

Figure 4: Cyclic Redundancy Check

2. Objective of the Work

Zigbee Transmitter can be designed with analog components. Designing an analog transmitter is easier than digital. But in analog design, data transmission will be poor and the components also bigger and more. This will not allow accurate data transmission. In designing with digital, accurate data transmission will be obtained and power supply voltage range will be smaller. One way of designing digital Zigbee transmitter is with the help of Verilog HDL and VHDL through Xilinx. The objective is to design and to synthesis the Zigbee transmitter using Verilog which will result in lesser numbers of slices and Look-up-Tables (LUTs) utilized and lossless data transmission. With lesser number of components the power utilized shall be reduced.

3. Design Methodology

The behaviour of the Zigbee digital transmitter can be modelled using VHDL through Xilinx ISE. The VHDL module for each transmitter can be combined, then synthesized, simulated, and implemented on Spartan3E FPGA. The input data comprise 22 symbols. Each data symbol from the bit-to-symbol block is append onto a 32-chip PN sequence using the DSSS method. The output data are 704 chips in total with the frequency of MHz. The numbers of chips produced are based on[88 bits/4] symbols x 32 = 704 chips Based on this equation, each even chip of output data is registered as C0, C2 ….. C704, and each odd chip is registered as C1, C3 …C703, which is totally 352 chips each for I-phase and Q-phase.

4. Results and Discussion

Simulation and implementation were performed for the digital Transmitter. The output waveforms were compared to verify their functionality. The simulation waveform shown in below Figure 5.

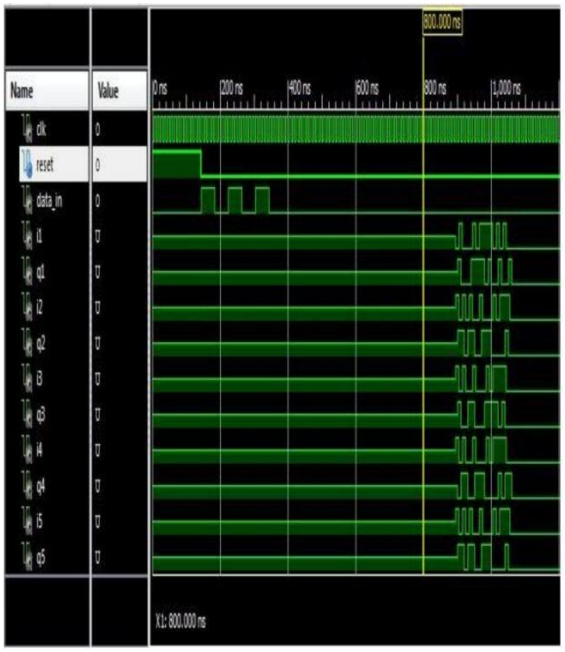

Figure 5. Simulation Waveform of Transmitter

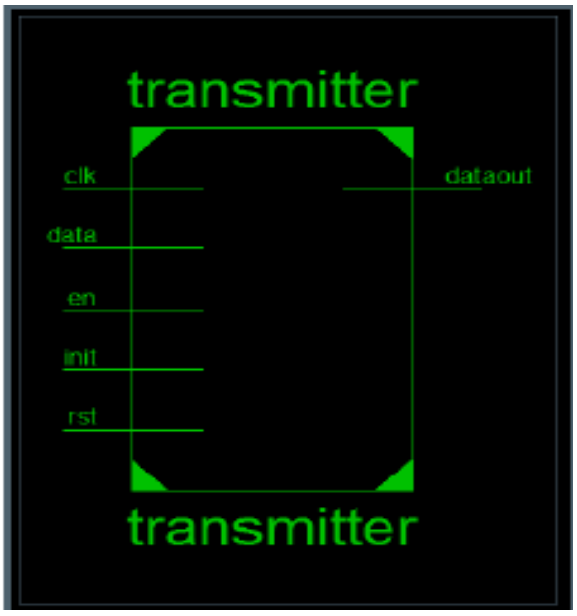

Figure 6. RTL View of Transmitter

5. CONCLUSION

This paper shows the Verilog based design of digital transmitter for 2.4GHz band Zigbee applications. The behavior of CRC and Bit-to-symbol were characterized using Verilog as well as using VHDL. From the discussion, so far, part of the Zigbee transmitter is alone is characterized and synthesized. Both the results and synthesis report were compared and discussion has made for the design methodology. The remaining part of the transmitter will be designed and synthesized in future.

REFERENCES:

[1] Sweatha Sankar T S, "Zigbee Standard Consists of a set of Communication Protocols for Wireless Networking"., 2016

[2] Anusha C.M, Kiran Kumare, "Implementation of a Digital Transceiver for 2.4 GHz Zigbee IEEE 802.15.4 Applications for a Given Acknowledgement" 2015.

[3] Punit Ramachandra Ramaji Manjunath G Asuti, "Design and Implementation of Zigbee Transmitter on FPGA using VHDL", 10th IRF International Conference, 01st June-2014, Pune, India, ISBN: 978-93-84209-23-0.

[4] Mohammed Mian A, Divyabharathi R. Design and simulation of Zigbee transmitter using Verilog. International Conference on Information Communication and Embedded Systems (ICICES); Chennai. 2013 Feb 21-22. p. 882–8.

[5] Somya Goel1, Dr Ranjit Singh, "Implementation of 2.4GHz-band Zigbee Transreceiver for an Acknowledgement Frame." 2013,

[6] Khalifa. O, Islam. MDR and Khan. S, "Cyclic redundancy encoder for error detection in communication channels", RF and Microwave Conference, 2004.

[7] Matloff N, "Cyclic redundancy checking", Department of Computer Science, University of California, 2001.

[8] Rafidah Ahmad, Othman Sidek, Wan Md. Hafizi Wan Hassin, Shukri Korakkottil Kunhi Mohd, and Abdullah Sanusi Husain, "Verilog-Based design and implementation of Design Tansmitter for Zigbee Applications", International Journal of Emerging Sciences, 723-724, December 2011, ISSN: 2222- 4254, © IJES.

[9] Rahmani. E, "Zigbee/IEEE 802.15.4", University of Tehran, 2005.

[10] Shuaib. K, Alnuaimi. M, Boulmalf. M, Jawhar. I, Sallabi. F and Lakas.A, "Performance evaluation of IEEE 802.15.4: Experimental and simulation results", Journal of Communications, 2, 4(2007): 29-37.

[11] Sunil Shukla, Neil W. Bergmann, "Single bit error correction implementation in CRC-16 on FPGA", Proceedings of IEEE International Conference on Field-Programmable Technology 2004.

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