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VLSI Implementation of FPGA based 8 bit Barrel Shifter

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ABSTRACT

Barrel shifter is a digital circuit that can move an information word by a predefined number of bits. Barrel shifters are applicable for digital signal processors. Several types of shifting operations exist depending on the target application, including shift logical, shift arithmetic and rotate. In this work a set of hardware design alternatives for shifters to perform the different types of shifting operations was analyzed, designed and implemented in a Virtex-4- FPGA. In arithmetic and logic operations barrel shifters is used to shift a desired number of bits in a desired direction. In this paper an 8-bit & an 16-bit barrel shifter architecture is proposed and implemented using Verilog code.

Keywords:— *barrel shifter, Multiplexer, rotate left, shifter, right shift, logical right, fpga.*

I. INTRODUCTION

A Barrel Shifter is a logic component that performs shift or rotate operations. Barrel shifters are applicable for digital signal processors. This component design is for natural size (4, 8, 16…) barrel shifters that perform shift right logical, shift left logical, rotate left and rotate right operations depending on the instantiation parameters. The left and right operation is implemented through inversion of the input and output vectors. The number of multiplexing stages is relative to the width of the input vector.

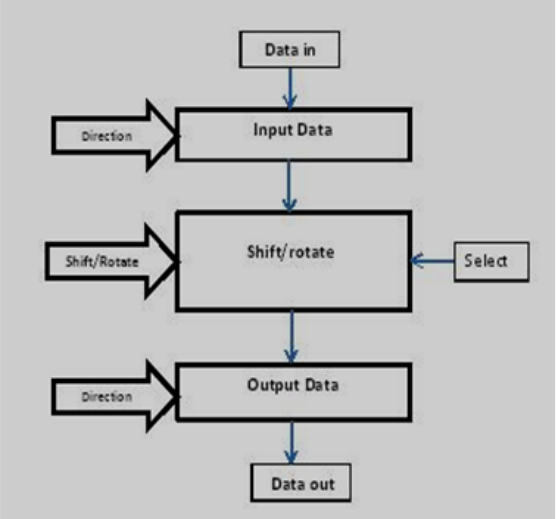

Figure 1. Block Diagram of Barrel Shifter

Shifting and rotating data is required in several applications including arithmetic operations, variable length coding, are bit indexing. Consequently, barrel shifters which are capable of shifting or rotating data in a single cycle. Select lines are used to specify the amount of shift only. A barrel shifter can be designed by using mux trees.

Architecture

1. Logical right shifter:

A logical right shifter using a fore mentioned approach is shown in the figure 1.The first row corresponds to a shift of one, while the last row

corresponds to a shift of four, As required, zeros fill the high order region. Hence, interconnects route zero into the high order multiplexers. The values x_amt[x] represents the bit in position x of the shift amount, and as such represents the value 2^x,

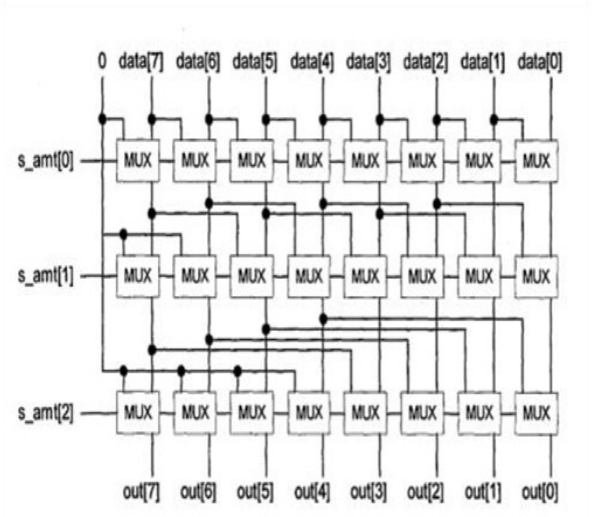

Figure 2. Logical Right Shifter

1.1 Operation of right shifter:

The shift right logical operation is much like a rotate right but without the lower order bits (LSB) being moved to a high order (MSB) position. Instead, the LSB bits are removed. The remaining bits are shifted to the right so as to fill the void created by the loss of the low order bits (LSB). The void created in the MSB region by this shift is filled with zeros.

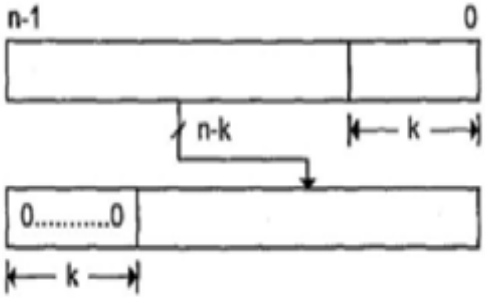

Figure 3. Right Shifter Operation

As shown in example below, the LSB bit is removed from the result and the remaining bits are shifter over. The order bits are set to zero.

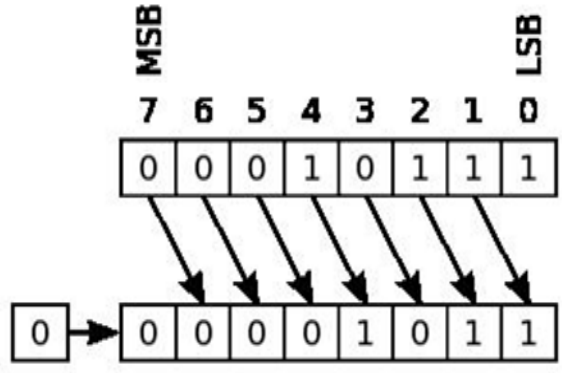

Figure 4. Example of right shifter

II. RIGHT ROTATOR

A right rotator is very similar to a logical right shifter. The differences between the two lies in the manner in which interconnect lines are placed, In particular, since all of the input bits are routed to the output, there is no longer a need for interconnect lines carrying the zero signal. Instead, interconnect lines need to be inserted to enable routing of the low order bits from each row to high order region so that rotate can occur. The longer interconnect lines of the rotator, however, can increase both area and delay.

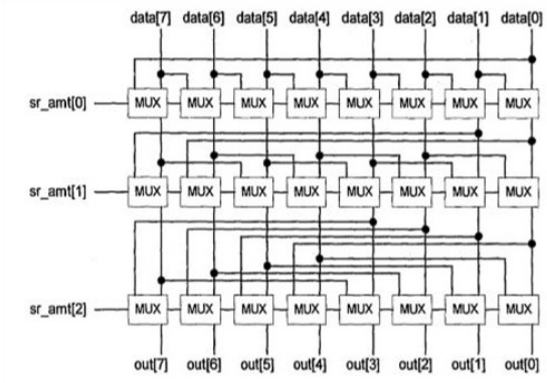

Figure 5. Right Rotator

2.1 Operation of right rotator:

Rotate is a cyclic shift either to the left or right. This means that as bits are shifted out of the data vector on one side, they are shifted into the data vector on the other side. During this process, all bits from the input are routed to the output. Their position in the output, however,

is not necessarily the same as it was in the input.

An example of rotate right can be seen in the figure 6 where a 8-bit word of data has a one bit rotated right.

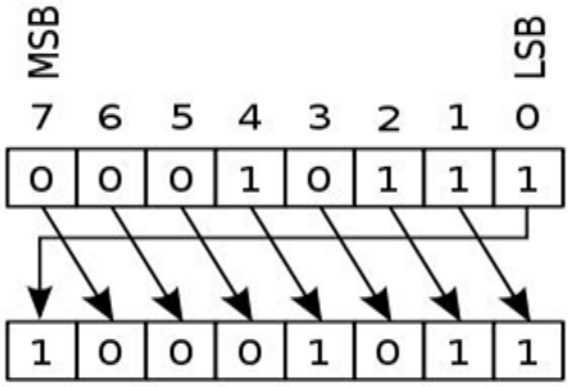

Figure 6. Example for right rotator

III. RESULTS

The following figures show the RTL schematics of 8-bit & 16-bit barrel shifter respectively.

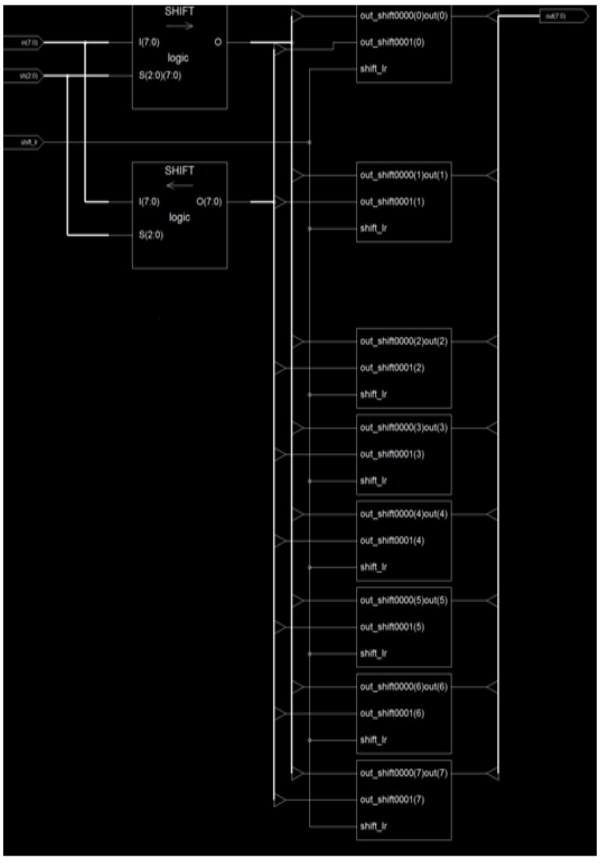

Figure 7. RTL schematic of 16-bit barrel shifter

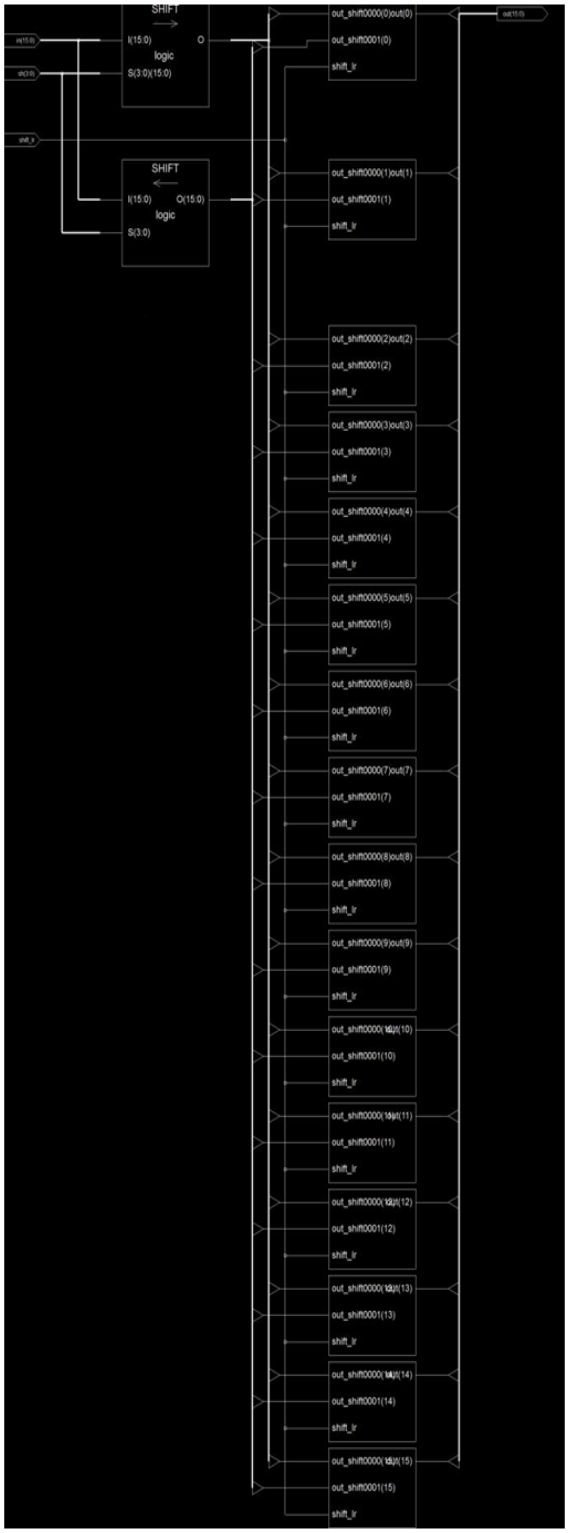

Figure 8. RTL schematic of 16-bit barrel shifter

The results shown below are for the 8 bit and 16 bit barrel shifter which shows output waveforms for different operations such as right shift and right rotate.

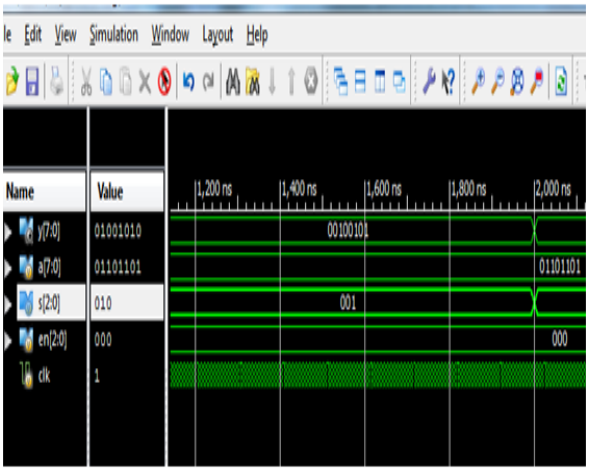

Figure. 9 Simulation wave form for 8 bit logical left shift

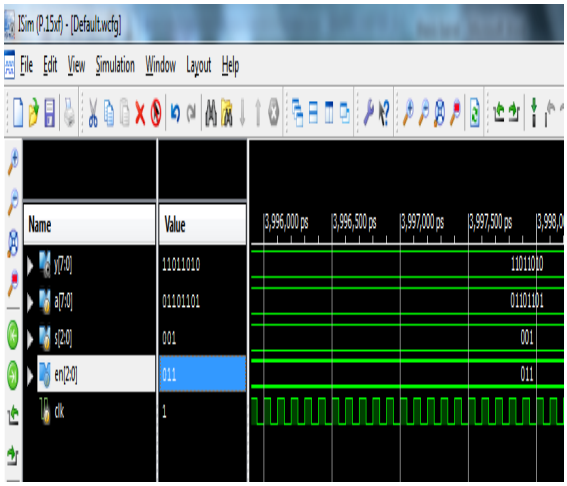

Figure 12. Simulation wave form for 8 bit rotate left shift

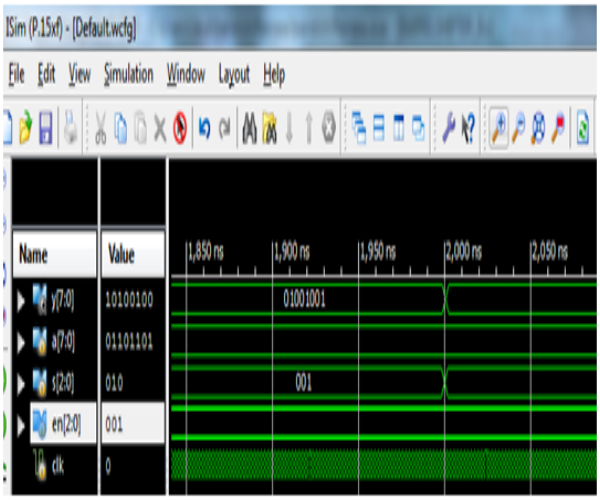

Figure 10. Simulation wave form for 8 bit logical right shift

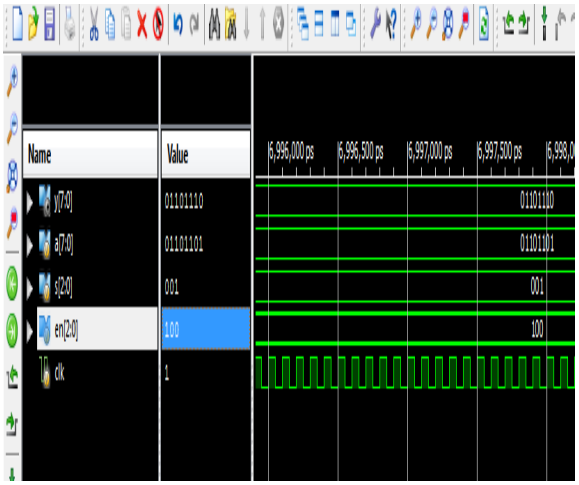

Figure 13. Simulation wave form for 8 bit airthmetic left shift

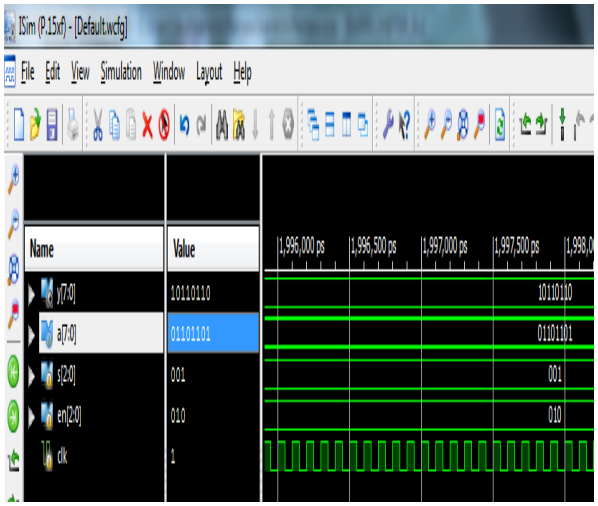

Figure 11. Simulation wave form for 8 bit rotate right shift

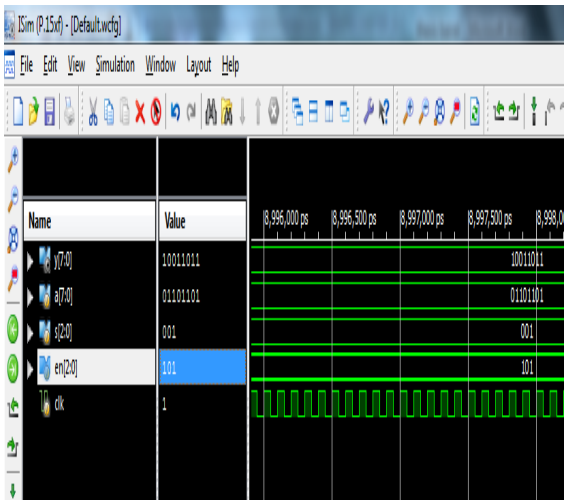

Figure 14 Simulation wave form for 8 bit airthmetic left right shift

Table 1- Design summary of 8-bit barrel shifter

Maximum Combinational Path Delay (in ns) for different Barrel Shifter at 8 Bit Level		
O. Anjaneyulu and T. Pradeep and K. Reddy 5	Sajib Kumar Mitra and Ahsan Raj Chowdhury	Result obtained
12.638	22	8.45

Table 2- Design summary of 16-bit barrel shifter

Maximum Combinational Path Delay (in ns) for different Barrel Shifter at 16 Bit Level	
Sajib Kumar Mitra and Ahsan Raj Chowdhury [1]	Result obtained
40	15.81

IV. CONCLUSION

We have proposed and designed a Verilog implementation of FPGA based barrel shifter. Which produce appreciable results. It demonstrated that our approach yields & High speed barrel shifter.

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