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# Estimation of High Performance Memristor Based 6T SRAM Cell

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***Abstract*—***In recent years, the demand for low power devices is increasing and the reason is the extension of CMOS technology. Due to the scale, the size of the chip is reduced and the number of transistors in the system on chip (SOC) is increased and this phenomenon is also true in the SOC memory. In general, the number of transistors used in the chip, to store data with respect to the number of transistors used for a different function. So in the future the need for an economy is to increase low power and low power memory capacity to design leaks is attentive to the design of the parameters of the low power device because they play an important role in the increase of the devices of overall consumption of energy. In this work, the static random access SRAM is designed for a type of semiconductor memory, a flip-flop circuit is used to store each bit. It is volatile in the traditional sense which is the loss of data when the memory is off. Memristor is used SRAMs to design and compare results with conventional SRAM. Design and calculation of simple SRAM parameters based on SRAM memristor was carried out with the Cadence tool, the technology is 45nm.*

***Keywords:—*** *6T SRAM, 4T SRAM, Memristor, Parameters, Implementation.*

## I. INTRODUCTION

In the future, the demand for portable devices such as cell phones, laptops, PDAs, tools and electronic systems is increasing in the field of notebooks. Low-power electronics, the system is added, and the system uses memory to store data. One type of SRAM memory. The SRAM cell does not need to be refreshed with the technical and volatile properties, which means that when connected to the power supply, the data is used as power data to cover other qualities of the SRAM by which the use of the transistor is lost to a bit on the system memory chip (SOC) Stored, and reduced latency memory between processors. These advantages of SRAM are used to develop portable systems, so low power SRAM is very demanding in portable devices, so this file is based on the memristor SRAM. This article is intended for 6T SRAM. Memristors are used to develop low-power SRAM. The memristor is a passive electrical element with two ends of the nonlinear variable resistor also known as the recall. The associated electrical load and the link magnetic flux are a certain time interval. The memristor resistance depends on the magnitude and polarity of the voltage applied to it. It has voltage and current, which is similar to the non-linear relationship between the memory devices. The use of simple SRAM memristor

technology reduces overall power and energy leakage.

## II. 6T SRAM Cell Operation

Static random access memory (RAM), which can save power, is always stored information. This is where they are needed, which does not require any power to store periodic soda data or non-volatile memory, flash memory, such as dynamic RAM (DRAM). The term "Random Access" refers to each array of cells in SRAM cells can be read or written in any order, regardless of which cell the last accessed.

6 transistors of SRAM cells, whose structure stores one bit of information, can be seen in Figure 1. The core of two CMOS inverters, in which each inverter Vout from the output potential to the input is fed to the other in the form V in. This feedback loop is stable to investors of relevant states.

Transistor access and word and bit string, WL and BL, and for reading or writing to cells. In the standby state, the word line is low, disabling the transistors of access. In this case, the investor is a complementary state. When the p-channel MOS transistor to the left converter is activated, the potential V1, out is high when the MOS transistor with the p-channel and the inverter 2 is turned off, Vr, out it is low.

In order to write the information is applied to the data and the reverse bit of the reverse data line (BL) is a bit string. Then the word high-voltage line is activated when the transistor is installed. As a little line drive is more powerful, you could say an inverter transistor. After the information is stored in the transistor the access investors can be turned off and the information of the investor is saved. To read the word, the string is activated, and the bit line is detected to activate the information of the access transistor.

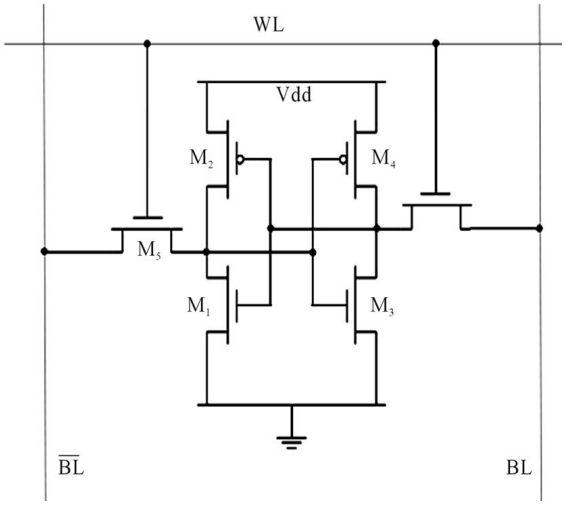


*Figure 1. Circuit Diagram of 6t SRAM Cell Operation*

## III. Read Operation

In the read operation, the word line controller is disconnected outside the word line is activated. This value can be determined if the inverter in the SRAM cell controls the external logic of the string bits. As a discharge line, the cell immediately after reading the recording operation was taken in the previous step with preload. In read mode, charge internal node and stable SRAM6T record If the investor is not strong enough "(the static margin of the noise immunity is too small), it can not be sufficiently discharged to the required value stored by the load scrambling of the bit string.

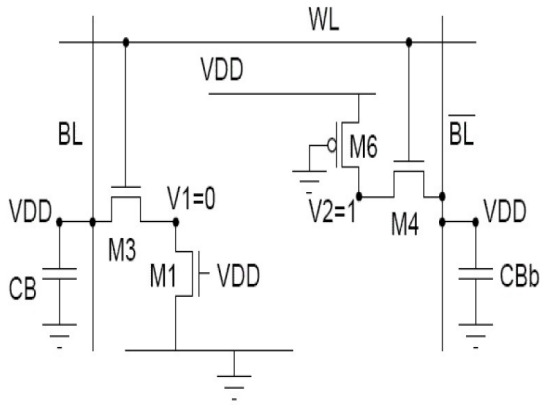


*Figure 2. Circuit Diagram of 6t SRAM Read Operation*

## 4. WRITE OPERATION

In the write operation, in order to increase the bit line, a large one with three driver states (external) must be activated. Existing couples can easily write a cross. This is because the internal controller (the small transistor 6T SRAM used by the base station) is much smaller than the external controller. Then it allows the word line of the transistor, however, shaft data, a short circuit occurs when only a few nanoseconds. The write data block is applied to the bit lines (B and B). Transistors of access (M3 and M4), applying the word line WL allowing signal to the gate "1". The line, when the data "0" is stored in the memory "1" storage node, then the corresponding bit equals the voltage is supplied to "0", so that the current through the extraction device (for example, PUP1) storage of the high storage node, it decreases. When the voltage of the storage node is higher than the other inverter (M6 pull-up and descent M2), the content is lower than the trigger movement due to the feedback unit. When the voltage of the storage node "0" and "1" should be written in reverse. If the first storage node stores "0", the row bit and the data "0", there is no change in the state of the battery. If the first node stores storage "1" in the bit string and data "1", then there is no change in the state of the cell.

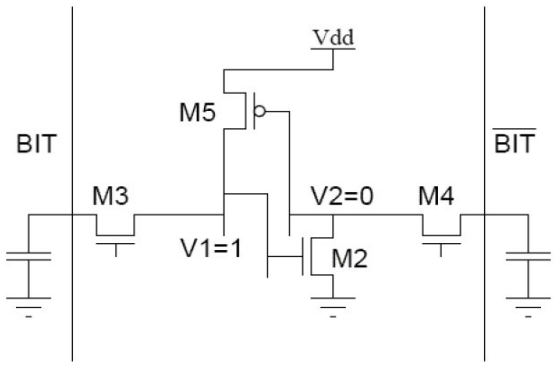


*Figure 3. Circuit Diagram of 6t SRAM Write Operation*

## V. MEMRISTOR

A memristor is a passive two-terminal element whose resistance is dependent on the magnitude and polarity of the voltage applied on it. It has a non-linear relationship between voltage and current, which is similar to a memory device.

Figure 4. Memristor

It gives relation between flux $(\phi m)$ and charge $(q)$ . A memristor is defined as one non-volatile two-terminal device in which the magnetic flux between the terminals is a function of the quantity and has been designated M by the charge Q and its Om block and mathematical similar ones –

$$M(q) = \frac{d\Psi m}{dq}$$

Where M is the Memristor, Φm is the magnetic flux and q is the charge.

## VI. MEMRISTOR BASED SRAM

SRAM get good results, but this type of memory, and the problem of data storage is, in fact, is unstable. In order to overcome such problems, new technologies to reduce power consumption and increase the speed of memory for reading/writing. In this article we develop on the basis of the memristor SRAM. The simple SRAM is variable in nature and thus increases the system start-up time and is based on the non-volatile memory of the SRAM memristor nature, so that historical data is stored and memory even when the power is turned off and maintaining these two states does not require a power source which, when The power supply is cut off according to data, holding a film based circuit without external memristor factors.

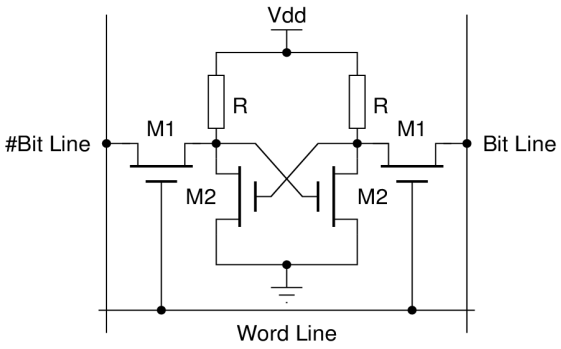


*Figure 5. Circuit Diagram of Memristor Based 6t SRAM*

A memristor as a switching transistor, except that the memory barrier is a two-terminal device and the transistor consists of three terminal devices. The memristor consists of two thin layers, and these layers are located between the nano wire and the platinum layers also on the nano meter scale. These layers of TiO 2-doped and un doped TiO 2 are different. The change in resistance, when the TiO 2 layer takes oxygen ions and other losses of TiO 2 layers of these layers of oxygen ions, that is, the motion of a charge of ions based on titanium dioxide changes the movement of the resistance layer of the memristor. That's why this is called variable resistance and the memory is designed for use. Therefore a pisastor can help reduce the overall power of the SRAM-based pisastor.

## VII. Power Dissipation

- Power dissipation system is classified into two curriculum:
- Static power dissipation and Dynamic power dissipation
- When the dynamic power consumption of the circuit is in the active state, that is, part of the work to complete the data.
- Since the capacities of a load-lifting
- When PMOS and NMOS are moderately active
- When the circuit is in the off state or in the static power dissipation occurs in the shutdown mode.
- Secondary transistor transmission in the mode of the downward threshold.
- Tunnel current through gate oxide
- In leakage currents of the diode reverse biased

$$\mathbf{Ptotal} = \mathbf{Pstatic} + \mathbf{Pdynamic}$$

$$\mathbf{Pdynamic} = \frac{1}{2}(\mathbf{CL} * \mathbf{VDD2} * \mathbf{fc})$$

$$\mathbf{Pstatic} = \mathbf{Ioff} * \mathbf{VDD}$$

Where,
CL= load capacitance
VDD=Power supply
fc= Clock frequency

Ioff =leakage current drawn by each switch in off state

## VIII. Leak Current Analysis

- In memory, we have many bits in the grid matrix. This characterized by the escape is a very important bit of the cell.
- The purpose of this analysis is to assist in characterizing the battery-bit column Drain.
- The main purpose of this test is to look at the amount of the margin
- During the read operation in a long column (unselected VNK).
- This analogue should serve as a guiding element, the maximum amount of design
- In the physical memory matrix.

To analyze the leakage current, it can be analyzed using bit cell

- q is initialized to Vdd.
- ˜q is initialized to 0.
- WL is OFF and therefore is set to 0.
- b and ˜ b is at Pre-charged.

The leakage current is measured as current through M3 (gateway NMOS transmissions for data 0).

(What if the leakage current is high: in this case, when we try to read the value Through cells of single-bit memory, we should not read the current value Other unselected cells a sufficient leakage current flowing through the ground Bt genes or BB lines, and therefore do not have the correct output value. )

Here, we have a technology for analysis of 45 nm.

Vdd is 1.1v.
Vss is 0v.

## IX. Speed

High-speed digital circuits can be found: delay

$$\mathbf{td} = \frac{(\mathbf{CL} * \mathbf{VDD})}{\mathbf{Ion}}$$

Maximum clock frequency:

$$\mathbf{fc\ max} = \frac{\mathbf{1}}{\mathbf{td} * \mathbf{Ld}}$$

Where, CL= load capacitance

$V_{DD}$=Power supply

Ion= Current leakage, drawn by each of the included states

Ld= logic depth (no of stages through which a switching events through the clock cycle)

## X. Leakage Reduction Techniques

In the emerging technology leakage reduction, some changes must process technology, phase / implementation production, to reduce leakage during development, while others are based on the requirements for building support for a scheme optimization program and in some cases, technical support, but are introduced during Execution (dynamically). Several methods discussed in this section of the level of leakage reduction schemes have been proposed, and are used to reduce the static energy consumption in the SRAM cell [4-10]

**Table 1. Comparison of 6t SRAM and 6t Memristor Based SRAM**

| | 6T SRAM (CMOS) | 6T SRAM (Memristor) |
|---|---|---|
| **Power** | 48.27E-9 | 15.63E-6 |
| **Leakage Current** | 5.550E-12 | 2.528E-12 |
| **Leakage Voltage** | 77.38E-3 | 650.8E-3 |
| **Delay** | 101.1E-9 | |

## XI. Advantages of CMOS Technology

Most often this is achieved by a SRAM cell that has the advantage of low static power consumption. However, the potential stability problems of such a design are such that, during the read operation, "0" can be stored with "1", the voltage in node V1 reaches Vth from NMOS N2 covered load node V2 is "0". In addition, additional nodes V1, rises to "1", because of the positive feedback mechanism.

- Production capacity
- Good margin of noise immunity
- Figured (in hazardous conditions, work reliably)
- Lower switching activity

## XII. Disadvantages

- It takes a lot of transistors
- Weak output processing
- Short-circuit power
- Power dissipation

## XIII. CONCLUSION

The proposed Memory is designed using 45 nm CMOS/VLSI technology with cadence. The Software used in program allows us to design and simulate an integrated circuit at physical description level. The proposed designed based on Memristor 6T SRAM. It is non-volatile in nature because of Memristor. It increases the packing density and reduces the power in system on chip (SOC) these techniques helps in reducing the leakage power in the device without loss of stored data. SRAM takes large part of power & area, therefore to improve power & speed here we are designing Memristor based SRAM.

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