



## **Performance of Three Phase Power Converter with Disturbance Attenuation Using Sliding Mode Control Approach**

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### **ABSTRACT**

*A novel scheme for the control of three-phase two level grid-connected power converters is presented in this paper. A cascade-control structure, based on  $H_\infty$  control and sliding mode control (SMC), is proposed, which simultaneously achieves output voltage regulation and unity power factor under dc-load variations. which comprises two control loops The overall control strategy contains two main loops: first, a current tracking loop (internal loop) based on sliding mode control that guarantees the input currents to follow the desired references; second, a dc-link voltage regulation loop (external loop) based on an  $H_\infty$  controller integrated with an extended state observer (ESO), which regulates the output voltage and provides current references for the internal loop. an  $H_\infty$  controller plus an ESO, which is designed to regulate dc-link capacitor voltage of the converter and asymptotically reject external disturbances and parameter perturbations Simulation results are provided to assess the efficiency of the proposed method.*

**Keywords:**— Three-phase power converters; Cascade control;  $H_\infty$  control; Sliding mode control.

### **I. INTRODUCTION**

Three-phase two-level power converters are popular power systems and provide several merits including high quality output voltage with small ripple, high power factor and quick current response and so on. In view of all these strengths, such converters have high industrial applications, for example adjustable speed drives, integration of renewable energy sources (RES) small current harmonic distortion, and bidirectional power used in modern energy conversion systems, such as ac drives, active frontends, reactive power compensation, active power filter, and battery charger used in hybrid electric vehicles (HEV). Particularly, in the application of HEV, it requires that the HEV must turn electrical power to mechanical power efficiently and economically while the utility current is ensured to draw a unity power factor to minimize line distortion. For this reason, the main control objectives are to regulate the output voltage to a desired one, supply a desired reactive power and ensure a power factor close to unity on the grid side again stparametric uncertainties and load perturbations. flow, etc. Particularly, in the application of RES, it requires that the power converters have relatively high efficiency, low installation cost and minimization of leakage current. To this end, during the past few decades, how to control of these power

converters to maintain the output DC voltage regulated to a desired value and draw grid currents with the lowest possible harmonic distortion has been extensively investigated by engineers and researchers [1].

Several control schemes have been put forward to control these power converters over the past decades [2]–[6]. Normally, the control of these systems is completed by using a cascaded structure. In such a structure, the internal loop is often accomplished by current controller, as well as the controller in the external loop regulates dc-link output voltage. For current tracking loop, different control methods have been studied in [7]–[9]. Early solution was linear proportional integral (PI) controller which has been widespread applied because of its reliability, strong adaptability and simplicity. However, it requires precise linear mathematical models and presents a slow dynamical response under parameter and load changes. Therefore, recently, some new control schemes have been proposed to solve these problems. Passivity-based control of three-phase two-level power converters was studied in [10]. A constant switching frequency algorithm of model predictive control current control (MPCC) has been applied in [11]. Input-output linearization and zero-dynamics control method was presented to control three-phase voltage-source converters in [12]. A flatness-based online trajectory planning algorithm has been introduced in [13].

It should be noted that among these control schemes, sliding mode control (SMC), a powerful nonlinear control approach, can well deal with the nonlinear behavior of the considered power systems due to its large-signal stability, fast dynamic response and complete robustness to matched disturbances [14]–[17]. Nevertheless, in conventional SMC, the control signal is discontinuous, which can produce the ‘chattering’ effect. Moreover, the high switching frequency not

only increase the losses but shorten the usable life of the power converters. The Gao’s reaching law approach is one of the most promising approach to reduce this undesired chattering effect [18]. It not merely reduces the system chattering but also forces the system states to reach the sliding manifold in finite time. Thus, based on Gao’s reaching law a sliding mode current controller is designed in the internal loop in this paper [19]. For dc-link voltage regulation loop, in most cases, the control method is often conventional PI control [20]. However, an equivalent resistive load regarding as an external disturbance has a great impact on the considered systems performance. In this paper, the Extended State Observer (ESO) is used for feed forward compensation to improve the transient performance. Although, ESO is an efficient observer to estimate an external disturbance, there always exists the estimation error which is considered as a disturbance error. To solve this issue,  $H_\infty$  control approach is applied in dc-link voltage regulation loop, which can diminish the influence of disturbance error on the power systems to its given level. The outline of the paper is as follows. Section II contains the model of power converter in dq synchronous reference frame and the statement of the control objectives. In Section III, a cascade-control scheme, based on  $H_\infty$  control and sliding mode (SMC) control, is presented. A realistic simulation is provided in Section IV to show the validity of the developed methods, and Section V gives some conclusions.

## II. MODELING OF POWER CONVERTER

Figure 1 shows a general schematic diagram of three-phase two-level grid-connected power converter, where  $e_a$ ,  $e_b$  and  $e_c$  are phase voltages  $L$  and  $r$  are the inductance of the input inductors and equivalent series resistance of the interconnecting reactors  $R_L$  is the equivalent load that can be regarded as

an unknown external disturbance  $C$  is the capacitance of output capacitor. The electrical circuit of the investigated power converter is presented where  $n$  stands for the neutral point. It presents a three-phase fully controlled bridge comprising six switching devices, which are connected to the grid through smoothing inductor  $L$ . The DC side consists of a load  $R$  load and a filter capacitor  $C$  connected with the load Through using the Park's transformation, the system dynamics of a three-phase two-level power converter can be expressed in dq synchronous reference frame as,

$$L \frac{di_{dq}}{dt} = -ri_{dq} + j\omega L i_{dq} + v_{dq} - v_{dqvc} \quad (1)$$

$$C \frac{d}{dt} \left( \frac{v^2}{2} \right) = v_{cu}^T dq i_{dq} - v^2 c / RL \quad (2)$$

Where  $i_{dq} = \{i_d, i_q\}^T$  is the inductor current;  $v_{dq} = \{v_d, v_q\}^T$  is the grid voltage vector;  $u_{dq} = \{u_d, u_q\}^T$  is the control input;  $v_c$  is the output capacitor voltage, and  $\omega$  is source grid voltage angular frequency

The above model mainly includes two dynamics inductor current dynamics and dc-link voltage dynamics. The main control objectives of the above power converters are stated as follows

- The quadratic current  $i_q$  should track its desired value  $i^* q$  to guarantee power factor close to unity (setting  $i^* q = 0$ ). Mean while, the direct current  $i_d$  should track a slowly varying reference signal  $i^* d$  generated by the voltage regulation loop

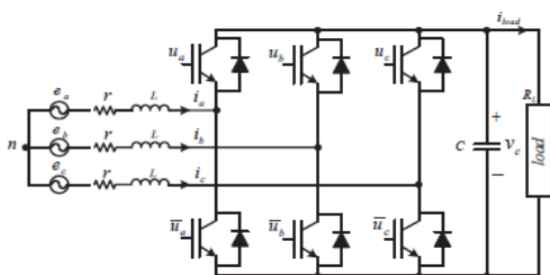


Figure 1. Synchronous rectifier based on the three-phase two level power converter

- The output voltage  $v_c$  should be regulated to a constant reference  $V_d$ , i.e.,  $v_c \rightarrow V_d$ . It should be noted that a current tracking loop (internal loop) and a dc-link voltage regulation loop (external loop) are required to achieve the above control objectives, respectively.

### III. CONTROL STRATEGIES

In this section, we concern with the control strategies for three-phase two-level grid-connected power converters. A cascade-control scheme, based on  $H_\infty$  control and sliding mode control, is presented to control the system (1)-(2). For the external loop (voltage regulation loop), an  $H_\infty$  controller combined with an extended state observer (ESO) is used to ensure the regulation of the capacitor voltages. For the internal loop (current tracking loop), a sliding mode controller is applied to drive the input currents to wards the desired values. A schematic block diagram of the control strategies is shown in Figure 2, where a PLL has been included to perform the Park's transformation [24]. A cascade control structure comprising an instantaneous power tracking loop and a voltage regulation loop, is put forward to control the power converter to achieve the above control objectives. In the voltage regulation loop, an ESO plus an  $H_\infty$  controller is designed for the regulation of the output capacitor voltage. Meanwhile, the outer loop provides the reference of instantaneous active power  $p^*$ , which is used in the power tracking loop.

#### 3.1 External loop

The control objective of external loop is to force the dc-link output voltage  $v_c$  to a desired reference  $V_d$ . To boost the controller design in the external loop, it is assumed that the current dynamics are much faster than the output voltage dynamics, thus, the dynamic of the output capacitor voltage is then given as follows,

$$\dot{z}_1 = \frac{1}{C} (p^* - pL) \quad (3)$$

where  $Z_1 = \frac{1}{2}v^2$ ,  $p^* = vcu^T dq i^* dq$  and  $PL = (v^2c)/RL$  that can be regarded as an unknown external disturbance. In order to asymptotically cancel the disturbance, the ESO is designed to improve disturbance rejection ability of system. First, extending the disturbance term as an additional state variable, i.e.,  $z_2 =$  then the system model (3) can be rewritten as

$$\dot{Z}_1 = up - z_2 \quad (4)$$

$$\dot{Z}_2 = d(t),$$

where  $up = \frac{P^*}{C}$  and  $d(t)$  represents the time derivative of  $z_2$  which is assumed to be a bounded function.

In view of the structure of the above model, the following linear ESO is proposed:

$$\hat{Z}_1 = up - \hat{Z}_2 + \rho_1(z_1 - \hat{Z}_1) \quad (5)$$

$$\hat{Z}_2 = -\rho_2(z_1 - \hat{Z}_1),$$

where  $\hat{Z}$  is the estimate of  $z =$  and  $\rho_1$  and  $\rho_2$  are positive parameters determining the bandwidth of the ESO.

Define the estimation error vector as  $\check{Z}$ , then its dynamics is represented as,

$$\check{Z}_1 = -\rho_1 \check{Z}_1 - \check{Z}_2, \quad (6)$$

$$\check{Z}_2 = \rho_2 \check{Z}_1 + d(t).$$

Then, the equation (6) is rewritten as,

$$\dot{\check{Z}} = A\check{Z} + \varphi(t) \quad (7)$$

where  $A =$  and  $\varphi(t) =$  Give that  $\rho_1$  and  $\rho_2$  are positive gains, thus it is easy to verify that  $A$  is a

Hurwitz matrix. According to [25], under the assumption that

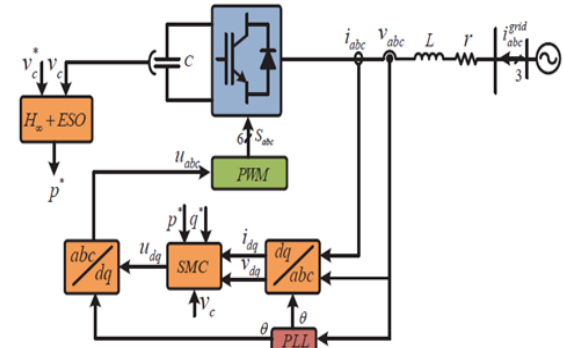


Figure 2. Proposed Cascade control Structure

$\varphi(t)$  is bounded, then there exists a positive constant  $\delta$  and a finite time  $T$  such that the state estimates in the system are bounded,

$$\|\check{Z}\| \leq \delta, \forall t \geq T. \quad (7)$$

Based on the estimated state  $\hat{z}_2$ , a state-feedback controller is designed as

$$up = K\varepsilon_1 + \check{Z}_2, \quad (8)$$

where  $\varepsilon_1 =$  is output voltage tracking error and the controller gain  $K$  will be designed via  $H_\infty$  technique. The dynamics of  $\varepsilon_1$  become

$$\varepsilon_1 = -K\varepsilon_1 + \check{Z}_2. \quad (9)$$

Next, we are interested in using the  $H_\infty$  technique to calculate the controller gain  $K$  in Eq. (8) for regulating capacitor voltage  $v_c$  in the presence of the disturbance input (estimation error  $\check{Z}_2$ ). It is well known that in [26] for giving performance level  $\gamma$ , by solving a group of linear matrix inequality (LMI), one can obtain an admissible controller  $K\varepsilon_1$ , which guarantees that the system (9) satisfies

1) The resulting dynamics of  $\varepsilon_1$  is asymptotically stable

with the disturbance input (estimation errors)  $\check{Z}_2 = 0$ ;

2) Under zero-initial condition, the following inequality

$$\int_0^{+\infty} \varepsilon 1^T(t) \varepsilon 1(t) dt \leq y^2 \int_0^{+\infty} \tilde{Z} 2^T(t) \tilde{Z} 1(t) dt \quad (10)$$

#### 4.2 Internal loop

A sliding mode current controller is designed in the internal loop to drive the input currents  $i_d$  and  $i_q$  to their desired values  $i^*d$  and  $i^*q$ , respectively. Define the current error as

$$\tilde{i}_d = i^*d - i_d, \quad (13)$$

$$\tilde{i}_q = i^*q - i_q,$$

where the desired value  $i^*d = p^*/v_d$  is calculated from the external loop to achieve voltage regulation, and the desired value  $i^*q$  is set to 0 to achieve unity power factor. Consider the first time derivative of  $\tilde{i}_d q = [\tilde{i}_d, \tilde{i}_q]$ ,

$$\begin{bmatrix} \dot{\tilde{i}}_d \\ \dot{\tilde{i}}_q \end{bmatrix} = \begin{bmatrix} \dot{i}^*d + \frac{r}{L} i_d - \frac{v_d}{L} - w i_q \\ \dot{i}^*q + \frac{r}{L} i_q - \frac{v_q}{L} + w i_d \end{bmatrix} + \frac{v_c}{L} \begin{bmatrix} u_d \\ u_q \end{bmatrix} \quad (14)$$

In order to force the current errors  $\tilde{i}_d$  and  $\tilde{i}_q$  to zero in finite time, the controllers  $u_d$  and  $u_q$  based on sliding mode control are designed as follows:

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = \begin{bmatrix} \frac{L}{v_c} (-V_d(\tilde{i}^*d) + \frac{v_d}{L} - \frac{r}{L} i_d - \frac{v_d}{L} - w i_q) \\ \frac{L}{v_c} (-V_q(\tilde{i}^*q) + \frac{v_q}{L} - \frac{r}{L} i_q - \frac{v_q}{L} + w i_d) \end{bmatrix} \quad (15)$$

where  $v_d$  ( $\tilde{i}_d$ ) and  $v_q$  ( $\tilde{i}_q$ ) are sliding mode current controller to be designed. Substituting (15) into (14), then (14) can be rewritten as,

$$\begin{bmatrix} \dot{\tilde{i}}_d \\ \dot{\tilde{i}}_q \end{bmatrix} = \begin{bmatrix} -v_d(\tilde{i}^*d) + i^*d \\ -v_q(\tilde{i}^*q) + i^*q \end{bmatrix} \quad (16)$$

Select the following sliding surface:

$$\sigma_{dq} \begin{bmatrix} \sigma_d \\ \sigma_q \end{bmatrix} = \begin{bmatrix} \tilde{i}^*d \\ \tilde{i}^*q \end{bmatrix} \quad (17)$$

Then, by using the reaching law approach in [18], one can

$$\text{obtain that, } \sigma^*j = -\epsilon_j \text{sign}(\sigma_j) - k_j \sigma_j, \epsilon_j > 0, k_j > 0, j \in \{d, q\}. \quad (18)$$

It follows from (17) and (18), one has

$$-v_j(\tilde{i}_j) + i^*j = -\epsilon_j \text{sign}(\sigma_j) - k_j \sigma_j, j \in \{d, q\}. \quad (19)$$

Moreover, the sliding mode current controller is designed as,

$$v_j = \epsilon_j \text{sign}(\sigma_j) + k_j \sigma_j + F_j, j \in \{d, q\}. \quad (20)$$

where  $|\tilde{i}^*d| \leq F_d$  and  $|\tilde{i}^*q| \leq F_q$  with some positive constants  $F_d$  and  $F_q$ . Hence,  $\tilde{i}_d q$  is steered to zero in finite time  $T_{dq}$  i.e.,

$$\tilde{i}_d = 0, t \geq T_{dq}. \quad (21)$$

it can be seen that the system is uniformly asymptotically stable. This completes the proof. gives the structure of the  $H_\infty$  control based on ESO voltage regulation loop designed.

Table 1. Simulation Parameter

Parameter	Value	Description
$f_2$	$5 \cdot 10^3$	Sampling Rate (Hz)
$f_3$	$5 \cdot 10^3$	Switching rate (Hz)
RL	30	Equivalent Resistive ( $\Omega$ )
C	3300	Capacitive Output Capacitive ( $\mu f$ )
L	2.3	Phase inductor (mH)
$f$	50	Grid frequency (Hz)
eabc	400	Grid line Voltage (V)
vdc	750	Capacitor Voltage Reference (V)



**Table 2.  $H_\infty$  Based SMC Controller Design Parameters**

Controller	Variable	Value
Internal Loop	$(\epsilon^*d, k_d, f_d)$	$(0.2, 10, 0.2)$
	$(\epsilon^*q, k_q, f_q)$	$(0.2, 10, 0.2)$
External Loop	$(y, K)$	$(0.12, 68.66)$
	$(\rho_1, \rho_2)$	$(6.0 \cdot 10^2, 3.6 \cdot 10^5)$

**Table 3. Adaptive Control Design Parameters**

Controller	Variable	Value
Internal Loop	$(K_{dp}, K_{di})$	$(10.2 \cdot 0.10^2)$
	$(K_{qp}, K_{qi})$	$(10.2 \cdot 0.10^2)$
External Loop	$(K_{cp}, K_{ci})$	$(0.7, 1705)$

#### IV. SIMULATION RESULTS

To verify the advantage of the proposed novel control scheme for three-phase two-level grid connected power converter in this paper, two simulation models (classic Adaptive control and the proposed  $H_\infty$ -based SMC) were accomplished by Matlab/Simulink. The design index and circuit parameter of the power converter system are shown in the Table I. In order to test the robustness of the proposed controller against load variation, a load step from no-load to a  $30 \Omega$  resistive load (18.75 kW) is applied at time  $t = 0.4$  sec.

The parameters of the proposed  $H_\infty$ -based SMC controllers are summarized in Table II, which are chosen such that the internal loop dynamics are much faster than that of the external loop. The welltuned parameters of Adaptive controller are given in III. It can be seen from Figure 3 that the period  $0 - 0.15$  sec is the pre-charge stage of the power converter and the controller is connected to the system after  $t = 0.15$  sec. In case of the proposed  $H_\infty$ -based SMC, the performance of the output capacitor voltage is indeed robust against load variation and has lower voltage overshoot compared with the PI control, i.e., the output capacitor voltage decreases by 17

V in case of the proposed  $H_\infty$ -based SMC, nevertheless PI control result is 30 V, after the load is connected (at  $t = 0.4$  sec).

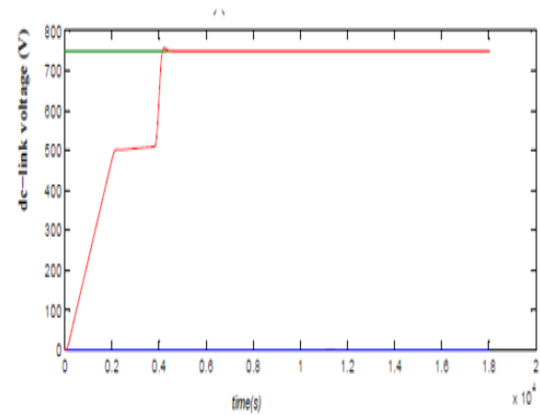


Figure 3. DC Link Capacitor (a)  $H_\infty$  based SMC (b) Adaptive control

Figures 4 and 5 illustrate the performance of direct current and quadrature current with their references in the presence of load variation. During the steady state, the direct current is maintained at 46.88 A, and the quadrature current is maintained at 0 A, so does the reactive power. The direct current and quadrature current errors are shown in Figures 6, which are in an acceptable range.

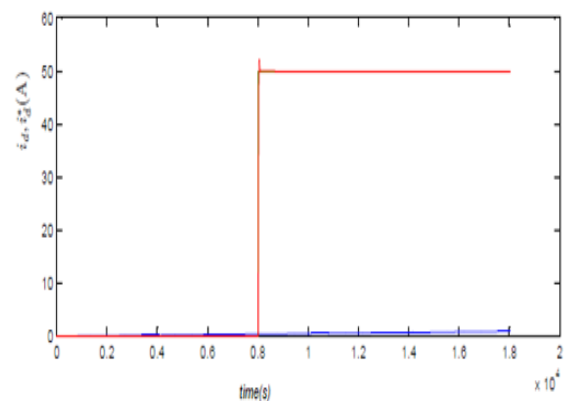


Figure 4. Curve of  $i_d$  and  $i^*d$  (a)  $H_\infty$  based SMC, (b) Adaptive Control

Figure 7 presents the source voltage (ea) with the corresponding phase current ( $i_a$ ) waveforms of the grid. In order to have clear graphs a gain of 0.15 was multiplied by value of the voltage.

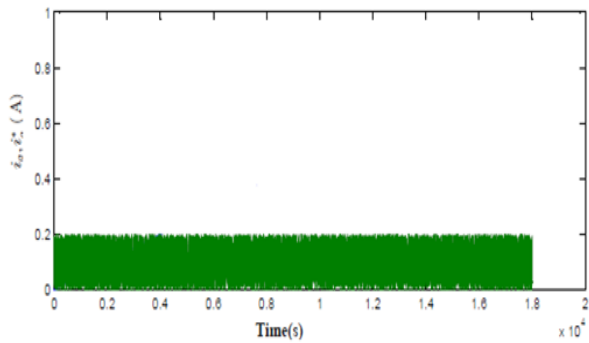


Figure 5. Curve of  $i_q$  and  $i^*q$  (a)  $H^\infty$  based SMC, (b) Adaptive Control.

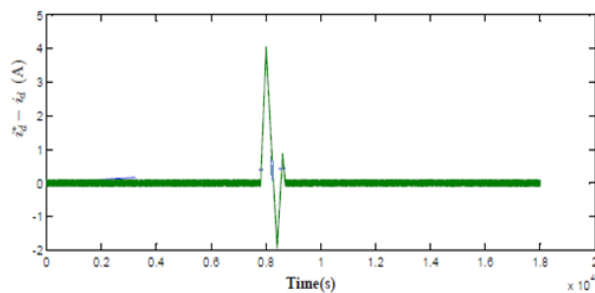


Figure 6. Direct and quadrature current error for the proposed control method.

There is no phase shift between the source voltage and corresponding input current of the both controllers as shown in the Figure 7, which means that the power converter works in near unity power factor mode. In fact, it should be noted that the total harmonic distortion value (THD) of the both proposed  $H^\infty$ -based SMC and adaptive control is 4.90% shown in Figure 8 in which the maximum frequency for THD computation is 6000 Hz. The corresponding dynamic responses of the ESO depicted in Figure 9 shows that the ESO has a good estimate of external disturbance.

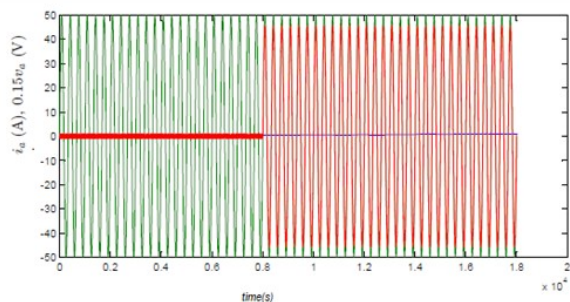


Figure 7. Phase current ( $i_a$ ) and grid voltage ( $v_{an}$ ) (a)  $H^\infty$  based SMC (b) adaptive control

## V. CONCLUSION AND FUTURE SCOPE

### Conclusions

In this paper, a novel control scheme for three-phase two-level power converters, based on the cascade implementation of  $H^\infty$  combined with sliding mode control, has been proposed. First, the modeling of three-phase two-level power converter in dq synchronous reference frame has been presented. The design of the controller has been detailed which is in cascade structure and comprises two control loops, i.e. current tracking loop (internal loop) and dc-link voltage regulation loop (external loop).

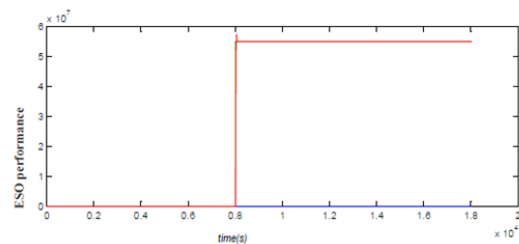


Figure 8 Curves of the  $Z1$  and  $Z2$

An  $H^\infty$  controller integrated with the linear ESO is designed to improve regulation transient performance of the capacitor voltage. A sliding mode current controller has been designed in the current tracking loop to force the input currents  $i_{dq}$  to track the desired values  $i^*_{dq}$ . The robustness and effectiveness of the proposed controller were confirmed through the simulation results.

### Future Scope

Future work will focus on the experimental validation of the proposed approach applied to the considered system and the extension to multilevel converters, such as neutral point clamped converters. Controller whose results can match with the required response in shorter time period. And concept. current tracking loop to force the input currents  $i_{dq}$  to track the desired values  $i^*_{dq}$ . The robustness

and effectiveness of the proposed controller were confirmed through the results.

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