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ASIC Realizations of a Distributed Arithmetic Reconfigurable FIR Filters of Higher Order

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ABSTRACT

Here with this paper, we project an effectual distributed arithmetic (DA) design for execution of digital FIR filter. The projected DA-based design utilizes the sharing method of the look-up table for the computing algorithmic terms i.e. filter outputs as well weight-increment. The quantity of the address is not in direct proportion to the with block size, while the quantity of the flip-flops are not at all dependent on the block size. Which is a crucialadvantage of the projected structure in order to reduce area, when a higher order filter is realized for larger block-sizes. ASIC synthesis result shows that, the anticipated structure for filter of higher orders, has almost 45.62% less area and 3.67% less power dissipation.

Keywords:—*Distributed Arithmetic Algorithm, Finite impulse response filter, High throughput, Look up table, Optimization.*

I. INTRODUCTION

Finite impulse response (FIR) digital filters play a vital role in various aspects of the digital signal processing (DSP) [1], [2]. With the time the digital signal processing is becoming prevalent, due to the excellent growth in very large scale integration (VLSI) technology. There is much demand of the he very higher speed FIR filters realization which consume less power. But as the filter order increases the complexity does increase too and there is the lag in real time operation and computation precision thus decreases, which leads to decrease in the accuracy level of the filter operation. So in order to get a dedicated structural design of the digital FIR filters in ASIC i.e. application specific integrated circuits lots of attempts have, therefore, been made. Distributed Arithmetic algorithm (DA) is a method which is used all over the world so that one can avoid using multipliers to implement sum-of-products computations. It has acquired even more admiration for the large throughput capability as well as regularity which has further resulted into area-time efficient and the cost-effective for computation [1].

DA is frequently used to form efficiently the Multiply-Accumulate Computation circuit (MAC) for various FIR filters and various Digital Signal Processing (DSP) applications. The high computational efficiency is the key benefit of DA [2]. The conservative multipliers are not required as DA allocates multiplication and accumulation operations through shifters, lookup-tables (LUT), and the adders. The DA code generation supports for the fixed-point filters designs only [3]. So distributed arithmetic can also be used for the higher

order filters. In order to improvise throughput, the simple DA algorithm is modified and it computes additional one bitwise sum at a time. The amount of instantaneously calculated bit wise sums is stated as a twos power termed the Distributed Arithmetic radix. The multipliers in MAC unit of many DSP functions have more power and area requirements. The LUT in Distributed arithmetic utilizes more memory. [7].

II. FIR FILTER DESIGN BASED ON DA

At an instant n, the outcome y[n] of an N-tap FIR digital filter with recent ingoing sample x[n] is given such as

$$y[n] = \sum_{i=0}^{N-1} w[i]x[n-i] \quad (1)$$

Where, w[i] (i = 0, 1, 2, 3, 4,……..., N − 1) signifies filter weights. Through signifying each and everyingoing samples i.e. x[n − i] in two's complement, we get

$$x[n\text{-}i] = x_{n-i} = -b_{i,B+1} + \sum_{j=1}^{B-1} b_{i,B-1-j}2^{-j} \quad (2)$$

By substituting (2) into (1) and rearranging, we get

$$y[n] = \sum_{j=0}^{B-1} c_{B-1-j}2^{-j} \quad (3)$$

$$\text{where } c_{B-1-j} = \sum_{i=0}^{N-1} w_i b_{i,B-1} \quad (j\neq 0)$$

$$c_{B-1} = -\sum_{i=0}^{N-1} w_i b_{i,B-1}$$

For a given set of w[i] (i = 0,1,2,3,4, ……...,N − 1), the terms cB−1−j would consider only one combination out of 2N probable combinations, which can be calculated well before and stacked in a look up table. The Distributed Arithmetic execution of a 4-tap Finite Impulse Response filter is represented in Fig. 1. At some extent the arriving bits of the input is stacked in particular order such as, the latest input samples are stacked in the topmost register whereas an old input sample is stacked in the bottom most register. The address line for the LUT is formed by the LSB of the registers which contains the partial product term. Afterwards these partial product terms are shifted and then accumulated for the "b" number of the clock cycles, which then produces the single sample output.

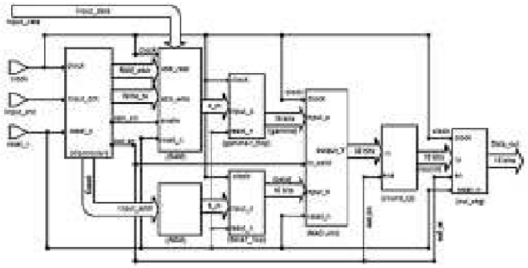

Figure1. Block diagram of the digital Filter using multipliers.

III. PROPOSED DA BASED FILTER

The anticipated configuration of the Distributed Arithmetic constituted FIR digital filter meant for ASIC application is as represented in Fig. 2. Input tasters {x(n)} coming on each sampling time are provided to a (SIPOSR) serial-in–parallel-out shift register having size N. The serial-in–parallel-out shift register (SIPOSR) crumbles N latest utmost samples towards P vectors bp of the length M for p = 0,1,2,3,4, ……...,P − 1 and provides these towards P reconfigurable partial product generators to analyze the partial products conferring to [19, 20]. For better-throughput execution, the reconfigurable partial product

generators(RPPG) creates L partial products conforming to L bit slices in parallel by utilizing the look up table poised of a very single register bank of 2M − 1 registers and L number of 2M : 1 MUXes [21].

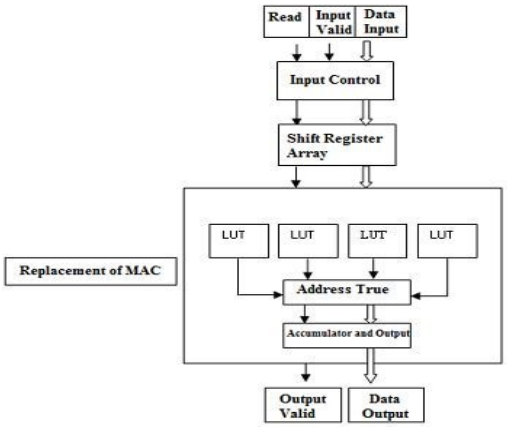

Figure 2. Bock Diagram of Implementation of FIR filter using DA

In the projected assembly, the reduced storing ingestion by means of involving each and every look up table across L bit slices is given. The register array is being chosen for this very perseverance rather than memory-based look up table, so that to access the Look Up Table contents at once. Along with, the fillings in register-based Look Up Table is able to get update in parallel in lesser cycles compared to the memory-based look up table to execute anticipated FIR filter [22, 23]. Width of each and every register with the look up table is $(W + \lceil \log_2 M \rceil)$ bits, whereas W is the word-length of filter coefficient. The input of the MUXes are 0, h(2p), h(2p + 1), and h(2p) + h(2p + 1); and the two-bit digit bl, p is fed to MUX l for $0 \leq l \leq L - 1$ as a control word. We can find that MUX l provides the partial product Sl, p for $0 \leq l \leq L - 1$ given by [20].In the figure 3 and figure 4 the higher order filters i.e. 64 and 128 of the proposed FIR filter design based on the distributed arithmetic is shown respectively.

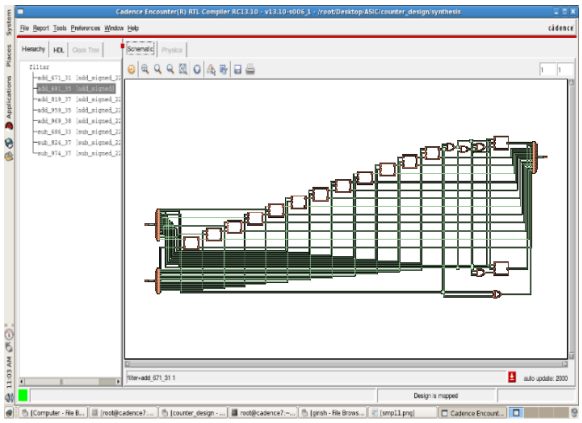

Figure 3. Proposed structure for 64-order FIR filter based on DA scheme

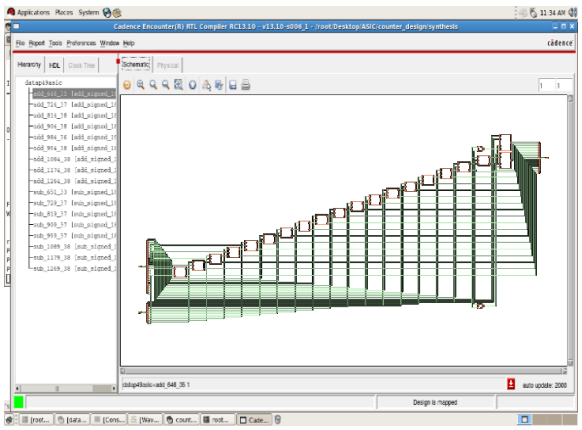

Figure 4. Proposed structure for 128-order FIR filter based on DA scheme

IV. Results and Discussions

The execution of FIR filter for ASIC implementation has been observed and validated, which refers that proposed fir filter structure compared to that of the DA based structure in [2], results are to be taken in terms of area utilized, the power dissipated as well as speed performance for 64bits and 128bits filter order. The anticipated assembly has smaller area as well as lesser power consumption quated with that of the Distributed Arithmetic-based structure [2].In fig.5 shows the results of the projected method as well as the earlier method by utilizing a 180-nm standard cell library. The anticipated structure uses less area on the chip level which shows that combinational logic is less used and thus reduce computation

complexity. As the logic blocks are reduced the power consumption is less and even the speed has been increased compared to that of the existing work.

Table 1: Performance Comparison For *L=M* =64

Parameters	[2]	Proposed	Proposed	Percentage Improvement
Filter Length	64	64	128	%
Area (sq.um)	24939	13563	25981	45.62
Power (nW)	67.23	15.71	31.73	3.27
Speed (ns)	6.81	1.1995	1.1992	4.67

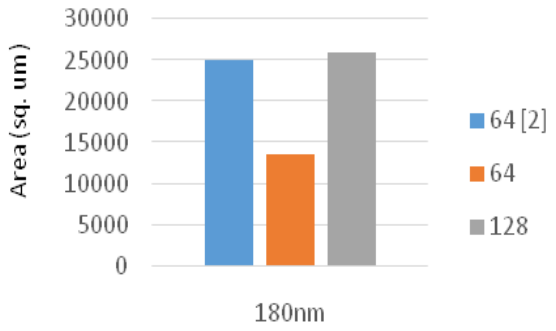

Figure 5. Area Comparison for 90 and 180nm technology.

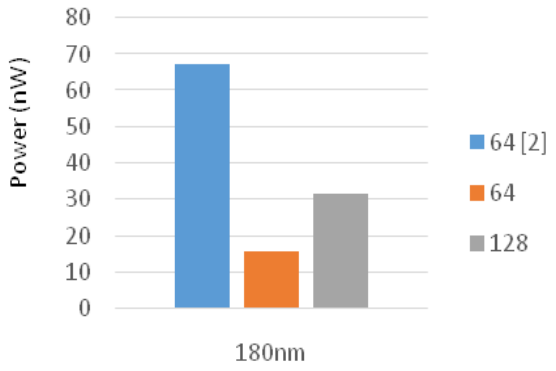

Figure 6. Power Comparison for 90 and 180nm technology

V. Conclusion

In this brief, an effectual structure aimed at higher order FIR digital filter for reconfigurable Distributed Arithmetic based ASIC application is presented. It has predicted that the structure hardware cost possibly will be determined by partaking the similar registers by means of the Distributed Arithmetic units meant for various bit slices. The projected plan has almost less area along with power consumption for the ASIC implementation. The design will able to be adopted to higher order filters. The percentage improvement in speed is 4 times, while power consumption is 3 times less and even area is decreased by 45%.

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